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Channel-Length-Modulated Avalanche Multiplication in Ambipolar WSe_2 Field-Effect Transistors

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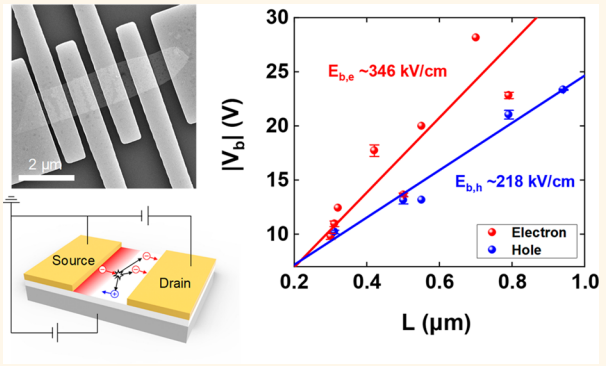
ABSTRACT: Recently there has been growing interest in avalanche multiplication in two-dimensional (2D) materials and device applications such as avalanche photodetectors and transistors. Previous studies have mainly utilized unipolar semiconductors as the active material and focused on developing high-performance devices. However, fundamental analysis of the multiplication process, particularly in ambipolar materials, is required to establish high-performance electronic devices and emerging architectures. Although ambipolar 2D materials have the advantage of facile carrier-type tuning through electrostatic gating, simultaneously allowing both carrier types in a single channel poses an inherent difficulty in analyzing their individual contributions to avalanche multiplication. In ambipolar field-effect transistors (FETs), two phenomena of ambipolar transport and avalanche multiplication can occur, and both exhibit secondary rise of output current at high lateral voltage. We distinguished these two competing phenomena using the method of channel length modulation and successfully analyzed the properties of electron- and hole-initiated multiplication in ambipolar WSe_2 FETs. Our study provides a simple and robust method to examine carrier multiplication in ambipolar materials and will foster the development of high-performance atomically thin electronic devices utilizing avalanche multiplication.



KEYWORDS: *2D materials, WSe_2, field-effect transistors, avalanche multiplication, ambipolar transport*

Transition metal dichalcogenides (TMDCs), a family of layered two-dimensional (2D) materials, are under extensive research due to their excellent electronic properties, light−matter interaction, and tunability of layer-dependent band gap.[1−5] Along with various device applications, there have recently been increasing reports of implementing avalanche multiplication in 2D materials.[6−14] Avalanche multiplication is a process where highly accelerated charge carriers collide with atoms and break free valence electrons to create additional electron−hole pairs in a chain reaction and has been utilized in ultrasensitive optoelectronic devices such as avalanche photodiodes and even single-photon avalanche detectors.[15] Moreover, device architectures such as impact ionization transistors have been realized to overcome the fundamental thermionic limit of transistors.[13,16] Recently reported devices utilizing 2D materials as active channels for photodetectors and transistors have exhibited ultrahigh performance,[12,13] which signifies the need for a deeper analysis of the fundamental physics and transport mechanism of avalanche multiplication in 2D materials. Although previous studies have examined the multiplication phenomenon, the experiments mainly focused on devising high-performance photodetectors, and the carrier type was limited to unipolar transport. However, ambipolar semiconducting materials that allow the charge transport of both carrier types (electrons and holes) in a single layer have great potential in device applications from memory and logic to light-emitting transistors.[17] In this regard, implementing avalanche multiplication in these ambipolar devices may provide another way toward high-performance electronics, and a detailed analysis of

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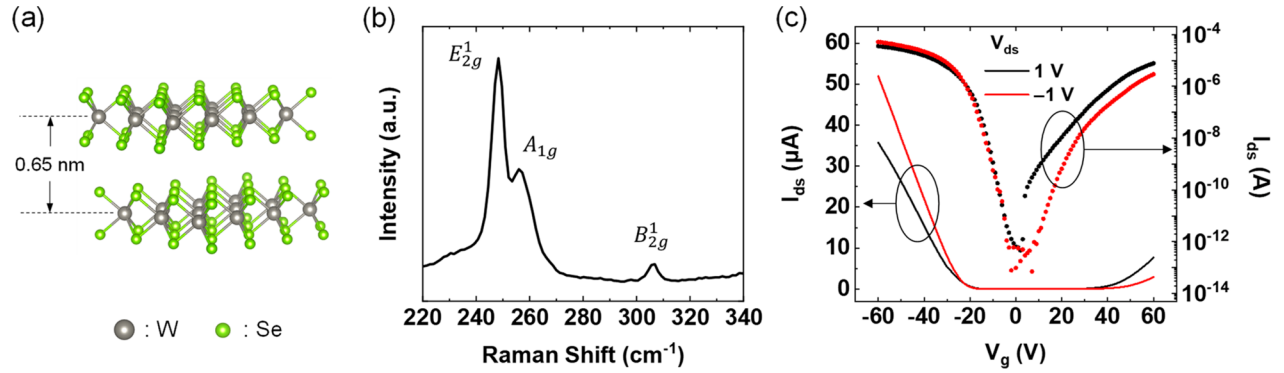

Figure 1. (a) Crystal structure of WSe_2. (b) Raman spectrum from a WSe_2 flake. (c) Transfer curves of a long-channel WSe_2 FET in linear and semilogarithmic scales exhibiting an ambipolar behavior.

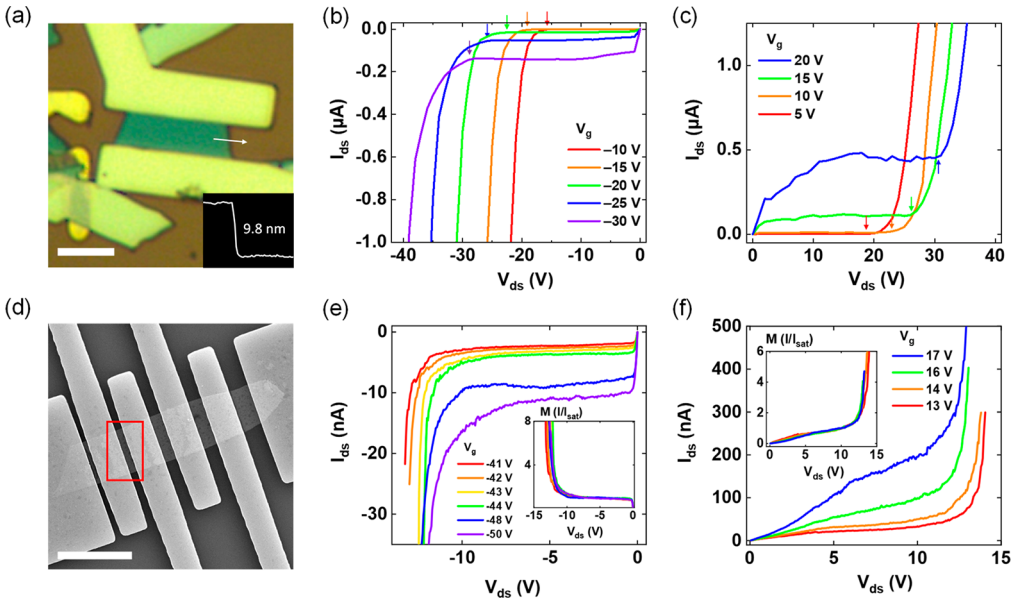

Figure 2. Comparison of electrical data from long-channel and short-channel WSe_2 FETs. (a) Optical image of a long-channel device. Scale bar: 5 μm. Inset is the AFM height profile of the flake showing a thickness of ~9.8 nm. (b, c) Output curves of the long-channel device in (b) p-type mode and (c) n-type mode exhibiting ambipolar transport characteristics. (d) FE-SEM image of multiple short-channel devices. The red box indicates the representative device. Scale bars: 5 μm. (e, f) Output curves of the representative short-channel device in (e) p-type mode and (f) n-type mode displaying avalanche multiplication. Insets are the plots of multiplication factor $M = I/I_{sat}$ corresponding to each output curve.

avalanche multiplication in ambipolar materials is highly desired.

In three-dimensional (3D) semiconductors, the impact ionization rates of electrons and holes are generally different from each other.[18−21] However, while ambipolar 2D materials such as WSe_2 are well known for their simple carrier type tuning *via* electrostatic gating in a field-effect transistor (FET) structure, the coexistence of both charge carriers in the channel hinders the separate analysis of multiplication by each charge carrier. Hence, there has been very little research in determining the impact ionization rates of ambipolar 2D materials. In this study, we investigated the multiplicative characteristics of ambipolar WSe_2 FETs. When an ambipolar material is used as the channel, the high drain−source voltage required to initiate avalanche multiplication causes an inversion of gating effect near the drain electrode, resulting in simultaneous ambipolar transport of both carriers through the channel.[22−25] This phenomenon is physically different from avalanche multiplication, but both are observed as an increase in output current after saturation, calling for the need to distinguish between the two phenomena. Focusing on the fact that ambipolar transport is governed by voltage, whereas avalanche multiplication by an electric field, we devised a method of channel length modulation to isolate the two competing phenomena and successfully analyzed the characteristics of avalanche multiplication in ambipolar WSe_2 FETs. We also compared the obtained results (such as breakdown voltages and ionization rates) from ambipolar 2D WSe_2 FETs with those previously reported on MoS_2 and 3D semiconductors with similar band gap energies.

RESULTS AND DISCUSSION

WSe_2 is an atomically thin semiconducting material, where each layer is separated by a van der Waals gap of ~0.65 nm (Figure 1a). We used a mechanical exfoliation method to transfer few-layer WSe_2 flakes onto a SiO_2/p++ Si substrate with an oxide thickness of 270 nm, then used the electron-beam lithography method to pattern source and drain

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electrodes (see Methods and Figure S1 in the Supporting Information for details). Pd with a thickness of 50 nm was deposited through evaporation as the electrode to provide efficient hole injection at the contacts.[26] The crystalline quality of WSe_2 was further examined using Raman spectroscopy (Figure 1b). The flakes used in the experiments showed the characteristic E^1_{2g}, A_{1g}, and B^1_{2g} peaks at ~249, ~258, and ~307 cm^{-1}, respectively, indicating interlayer vibrational modes in multilayer flakes.[27] Figure 1c shows the transfer curves (drain–source current *versus* gate voltage, I_{ds}–V_g) of a representative WSe_2 FET device. The measurement data showed good ambipolar electronic characteristics, exhibiting a high on–off ratio of ~10^7 for electrons and ~10^8 for holes. Field-effect mobility values for electrons and holes extracted from the data shown in Figure 1c were determined to be μ_e = 13.9 $cm^2/V{\cdot}s$ and μ_h = 37.3 $cm^2/V{\cdot}s$, respectively, using the formula $\mu = \left(\frac{\partial I_{ds}}{\partial V_g}\right)\frac{L}{WC_iV_{ds}}$ with a channel length (L) = 3.2 μm, channel width (W) = 9.9 μm, and capacitance per unit area (C_i) = 1.3 × 10^{-8} F/cm^2.

When sufficiently high voltage is applied between drain and source electrodes, metal-oxide–semiconductor FETs (MOSFETs) typically enter the saturation region due to the pinch-off near the drain electrode.[28] However, when the voltage is increased further, various physical phenomena can occur in the semiconductor channel. Here we demonstrate that modulating the channel length of a WSe_2 FET can change its transport characteristics under high voltage and explain further the two competing mechanisms. Figure 2a shows the optical microscope image of the long-channel FET device presented in Figure 1c. The thickness of the WSe_2 channel was measured to be ~9.8 nm. Figures 2b and c illustrate the dynamics of the device under high drain–source voltage in p-type and n-type modes, respectively. The output curves (drain–source current *versus* drain–source voltage, I_{ds}–V_{ds}) clearly exhibit triode and saturation regions at low drain–source voltage. As the drain–source voltage exceeds a particular value, the current rises further from its saturation level. This is in support of ambipolar transport and has been reported in FET systems with various channel materials.[17,22−25] The device operates by majority carriers up to the saturation point, and the secondary rise of current after the saturation is due to the accumulation of opposite charge carriers (*i.e.*, minority carriers) near the drain electrode (see Figure 2c). Since accumulation occurs similarly to how depletion occurs during the pinch-off, the current–voltage relation at this region is also parabolic in shape (see Figure S2 in the Supporting Information). Consequently, the current can be modeled by the following equations.[17]

$$I_{uni} = \frac{\mu_1 C_i W}{L}\left\{(V_g - V_{th,1}) - \frac{V_{ds}}{2}\right\}V_{ds}$$

in unipolar region where $|V_{ds}| \le |V_g - V_{th,1}|$ (1)

$$I_{sat} = \frac{\mu_1 C_i W}{2L}(V_g - V_{th,1})^2$$ in the saturation region where

$|V_g - V_{th,1}| \le |V_{ds}| \le |V_g - V_{th,2}|$ (2)

$$I_{ambi} = I_{sat} + \frac{\mu_2 C_i W}{L}\{V_{ds} - (V_g - V_{th,2})\}^2$$

in ambipolar region where $|V_{ds}| \ge |V_g - V_{th,2}|$ (3)

In eqs 1, 2, and 3, I_{uni}, I_{sat}, and I_{ambi} denote the output currents in the unipolar, saturation, and ambipolar region, respectively. V_{th} is the threshold voltage, and the subscripts 1 and 2 stand for electron and hole for the $V_{ds} > 0$ case, respectively, and *vice versa* for the $V_{ds} < 0$ case. The detailed explanation on the effect of V_g on ambipolar transport is illustrated with band structures in the Supporting Information (Figure S3). Additional measurements with devices of various WSe_2 thicknesses and channel lengths that exhibit similar current behavior are presented in the Supporting Information (Figure S4).

Although the ambipolar transport of TMDC materials at high voltage has been discussed in previous literature, our experiments suggest characteristics of another phenomenon dominant in the transport behavior when the channel length is shortened to submicron scales. Figure 2d illustrates an image of multiple short-channel devices fabricated on a single WSe_2 flake, taken with a field-emission scanning electron microscope (FE-SEM). The thickness of similar WSe_2 flakes as shown in Figure 2d was estimated as ~5.3 nm. The transfer curves of these devices are illustrated in Figure S5 in the Supporting Information. The output curves of both p-type and n-type transport of the representative device (marked by the red box) are plotted in Figure 2e,f. Note that even though this device has a shorter channel length than the long-channel device above, its current density was lower because of other factors such as thickness, contact, and interface conditions.[30]

Even though the transfer curve of this device exhibits ambipolar behavior similar to the long-channel device in Figure 2a, the output curves at high voltages are considerably different, indicating that the underlying physical mechanism is different in the short-channel transistor. As the drain–source voltage was increased after the saturation region, there was also a secondary rise of current until the measurement was stopped to prevent device failure due to thermal breakdown (see Figure S6 in the Supporting Information). Contrary to ambipolar transport occurring in a long-channel FET, the secondary augmentation of the current did not begin at different voltages. Instead, the current multiplied at a similar rate from its saturation value regardless of the gate voltage, as shown by the multiplication factor $M = I/I_{sat}$ values in the insets of Figure 2e and f (also see Figure S7 in the Supporting Information for other devices exhibiting similar behavior). There are some potential causes for the increase of current after saturation such as Joule heating at the contact or the current crowding effect.[29,30] However, considering that the current increase occurred at a low current level and that there was negligible dependence on the gate voltage, we ascribe this phenomenon to avalanche multiplication, and its characteristics are discussed in more detail later in the paper.

The contrasting shapes of output curves at a high voltage between the long- and short-channel devices are results of two distinct physical phenomena occurring in the channel. We define long-channel FETs as those that exhibit ambipolar transport (*i.e.*, parabolically increasing drain-current after saturation), where it is natural to define a critical voltage V_{cr} as the onset of the ambipolar transport (marked arrows in Figure 2b and c). Alternatively, short-channel FETs are those that display characteristics of avalanche multiplication, and we define a breakdown voltage V_b as the point where avalanche breakdown is attained (see Section 8 in the Supporting Information for determination of breakdown voltages). The critical voltages of various long-channel FETs and breakdown

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voltages of various short-channel FETs are summarized in Figure 3a and b for p-type (negative V_g) and n-type (positive V_g), respectively. Here, V_{cr} values of long-channel devices, depicted by blue open circles, exhibited a linear dependence on the modulation of gate voltage for both p-type and n-type. Moreover, the slopes of the fit lines were approximately equal to 1 for all devices, indicating ambipolar transport as expressed in eq 3, where $V_{cr} = V_g - V_{th,2}$. Note that the value of V_{cr} is independent of channel length, but dependent on the threshold voltages of either polarity. Thus, it is influenced by the dielectric constant of the insulator and interface conditions that affect the threshold voltage. The thickness and channel dimensions of these devices are summarized in Section 9 in the Supporting Information.

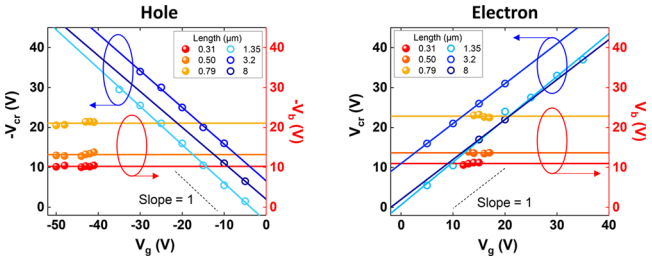

Figure 3. Critical voltage (V_{cr}) of long-channel devices and breakdown voltage (V_b) of short-channel devices for (a) p-type (negative V_g) and (b) n-type (positive V_g). V_{cr} values are represented with blue open circles, while V_b values are represented with red filled circles. The fit lines for long-channel devices have slopes close to 1 (shown in dotted lines), which indicates ambipolar transport.

On the other hand, breakdown voltages of short-channel devices were not strongly affected by the gate voltage but stayed nearly constant regardless of the applied V_g (Figure 3). In an atomically thin channel, the vertical movement of carriers is negligible, and the magnitude of applied V_g has little effect on the kinetic energy of charge carriers. Hence, modulation of V_g only changes the overall carrier concentration but not the multiplicative behavior. Instead, the V_b values increased with channel length, which is an indication that the mechanism of the observed breakdown phenomenon is related to the lateral electric field in the channel.

The channel length differentiating between long-channel and short-channel devices was approximately 1 μm in our WSe_2 FET structure. However, this transition point will be changed depending on the device structure. For example, using a thicker SiO_2 or other dielectrics with a low dielectric constant will weaken the ambipolar transport and allow avalanche multiplication even in longer channels. In contrast, using high-k dielectrics or ionic gels will induce accumulation of ambipolar charge carriers from very low voltages, and the channel will be overly conductive before avalanche multiplication can be observed.[24] Hence, using low-k dielectrics will be more suitable for the research of avalanche multiplication in 2D materials. In the transition region where avalanche multiplication and ambipolar transport are both possible, it is difficult to predict the exact transport characteristics, and further research would be desired.

The output current behavior and the transport mechanisms of long-channel and short-channel devices are explained in terms of energy band diagrams (Figure 4). For simplicity, the discussion in this section considers the n-type case with positive V_g and V_{ds}, where electrons act as the primary charge carriers at low voltage and holes start to accumulate as the voltage is increased into the ambipolar region. The opposite case holds similarly with negative V_g and V_{ds} applied to the device (see Figure S8 in the Supporting Information). Figure 4a depicts a schematic of the long-channel FET, including circuitry showing grounded source and high applied V_{ds}. When $V_{ds} > V_g - V_{th,h}$, charge accumulation in the WSe_2 channel takes the form as shown by red- and blue-shaded areas. Assuming a uniform channel resistance without consideration of defects and interface traps, the voltage across the channel can be modeled as a linear function $V(x) = V_s + x/L(V_d - V_s)$, where V_s and V_d are the voltages applied to the source and drain electrode, respectively, and x is the distance from the source electrode. Electron concentration at position x is then determined by $n(x) = C_i\{V_{g\_eff} - V_{th,e}\}/e$, where e is the electron charge and $V_{g\_eff} = V_g - V(x)$ is the effective gate voltage at each position. Electrons are accumulated near the source electrode, but decrease in concentration along the channel. Near the middle of the channel where $V(x) \cong V_g - V_{th,e}$, electrons are totally depleted. However, close to the drain electrode, V_{g_eff} becomes negative and eventually reaches the condition $V_{g\_eff} < V_{th,h}$. From this position of $V_{g\_eff} < V_{th,h}$, holes start accumulating and hole concentration becomes larger toward the drain electrode.[22] In this region, the hole concentration can be determined similarly to electron-rich region as $p(x) = C_i\{V_{th,h} - V_{g\_eff}\}/e = C_i\{-V_g + V_{th,h} + V(x)\}/e$.

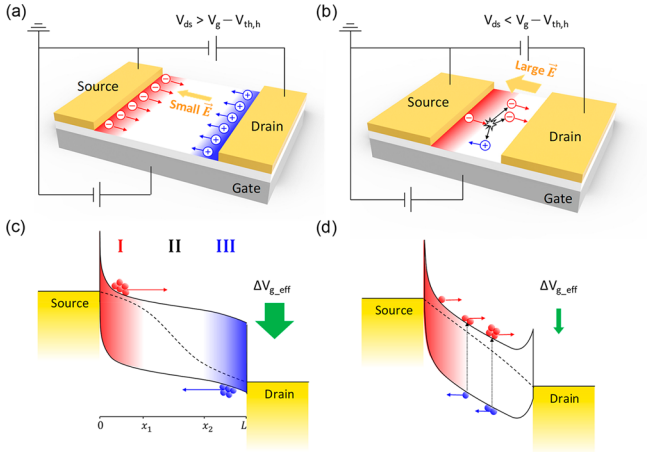

Figure 4. (a) Schematic diagram of a long-channel device in n-type operation mode during ambipolar transport. Electrons (red circles) are accumulated near the source electrode due to positive gate voltage. Holes (blue circles) are accumulated near the drain electrode due to the inversion of effective gate voltage (V_{g_eff}). (b) Schematic diagram of a short-channel device in n-type operation mode showing electron-induced avalanche multiplication inside the channel. An initial electron collides with an atom to create an electron−hole pair, and the charge carriers are subsequently accelerated in opposite directions by the applied electric field. (c) Band structure of the channel in the long-channel device during ambipolar transport. Electron-rich (region I), depletion (region II), and hole-rich (region III) regions are denoted in red, white, and blue, respectively. (d) Band structure of the short-channel device during avalanche multiplication. Fermi level throughout the channel is drawn with a dotted curve in (c) and (d).

The corresponding energy band diagram in the channel is described in Figure 4c, where the regions I, II, and III represent electron-rich, depletion, and hole-rich regions,

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respectively. The preceding analysis of charge carrier density with respect to position can be represented with varying Fermi level E_F. At each position in the channel, E_F can be expressed in terms of either n or p as $E_F = E_i + kT \ln(n/n_i) = E_i - kT \ln(p/n_i)$, where E_i is the intrinsic Fermi level, n_i is the intrinsic carrier concentration, k is the Boltzmann constant, and T is the temperature. By substituting the previously acquired formulas for $n(x)$ and $p(x)$, E_F near each end of the channel is expressed as

$$\text{Region I } (0 < x < x_1): \; E_F = E_i + kT \ln\left[\frac{C_i\{V_g - V_{th,e} - V(x)\}}{n_i e}\right], \text{ where } V(x_1) = V_g - V_{th,e} \tag{4}$$

$$\text{Region III } (x_2 < x < L): \; E_F = E_i - kT \ln\left[\frac{C_i\{-V_g + V_{th,h} + V(x)\}}{n_i e}\right], \text{ where } V(x_2) = V_g - V_{th,h} \tag{5}$$

In region II ($x_1 < x < x_2$), the effective gate voltage is between $V_{th,e}$ and $V_{th,h}$ such that both charge carriers are below the threshold. In this case, n and p are determined by the subthreshold diffusion model as $n = n_i \exp\left(\frac{e\{V_g - V(x)\}}{\eta kT}\right)$ and $p = \frac{n_i^2}{n}$, where η is the subthreshold ideality factor, leading to $E_F = E_i + e\{V_g - V(x)\}/\eta$. The Fermi level throughout the channel is drawn as a dotted curve in Figure 4c. The modulation of V_{g_eff} near the drain electrode also affects the band bending at the channel–electrode interface. As the Fermi level moves downward close to the valence band, the Schottky barrier is also reduced significantly, as illustrated by the green arrow.

On the contrary, the dominant process occurring in the short-channel devices at high drain–source voltage is different from long-channel devices. Figure 4b depicts a schematic diagram of the short-channel WSe_2 FET under high drain–source voltage. A high lateral electric field is created at relatively low V_{ds}, enough to induce avalanche multiplication before reaching the critical voltage for ambipolar transport. As the large electric field accelerates electrons, they gain enough energy to knock off bound electrons from atoms upon collision, generating electron–hole pairs. These newly created charge carriers are subsequently accelerated in opposite directions and undergo the same operation in a chain reaction, resulting in the avalanche breakdown.[31] It is notable that while avalanche multiplication had been traditionally studied in p–n junctions based on 3D semiconductors, many reports have successfully demonstrated the phenomenon and its application in photodetectors using an FET structure with 2D materials and metal electrodes.[32]

It has been previously studied in the case of bulk semiconductors that electrons and holes generally contribute to impact ionization at different rates.[18−21,33] To accurately determine the ionization rate of each carrier type, many experiments controlled the initial conditions to allow only unipolar injection in bipolar transistors or diodes.[33,34] In our experiment, the unipolar carrier injection was accomplished through electrostatic gating, which allows only one type of carrier to be injected from the source electrode. The corresponding band structure is illustrated in Figure 4d. The high electric field in the channel is portrayed as a steep slope of the conduction and valence bands. In the n-type operation where $V_g > 0$, E_F of the channel near the source electrode is close to the conduction band minimum, allowing the injection of electrons. Toward the drain electrode, V_{g_eff} is lowered, and pinch-off occurs similarly to long-channel devices. However, before the drain voltage is increased enough to induce the accumulation of holes, avalanche multiplication occurs throughout the channel. Here, the modulation of effective gate voltage is small, so the band bending at the interface and the height of the Schottky barrier are reduced by a small amount, as illustrated by the green arrow in Figure 4d.

The resulting parameters of avalanche multiplication that can be extracted for the WSe_2 FETs are analyzed in Figure 5.

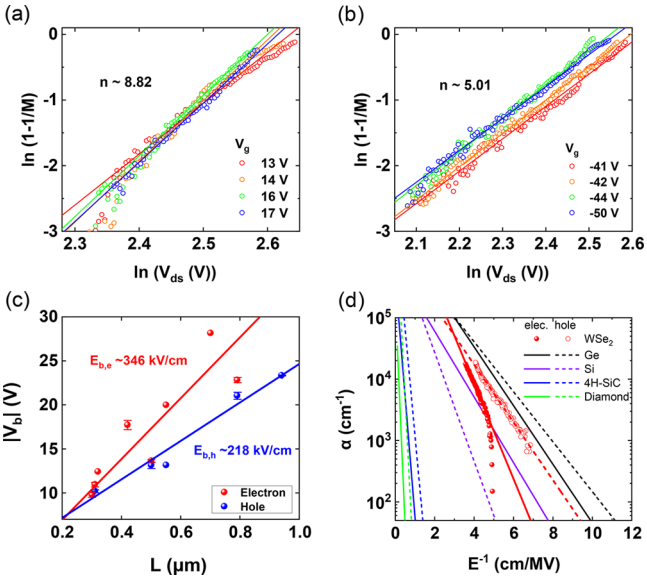

Figure 5. Characteristics of avalanche multiplication. (a, b) Logarithmic plot of $1 - 1/M$ *versus* V_{ds} in (a) electron-induced and (b) hole-induced avalanche multiplication. n is the ionization index. (c) V_b values as a function of channel length for n-type and p-type operation modes. The slope is the breakdown field for electrons ($E_{b,e}$) and holes ($E_{b,h}$). (d) Ionization rates (α) of electrons and holes as a function of inverse electric field for various materials.

The primary parameter is the multiplication factor M, which is directly acquired from the current–voltage (I–V) measurements. M is known to follow an empirical formula, $1 - 1/M = (V/V_b)^n$ where n is the ionization index, for conventional semiconductors, such as Si[19] and Ge,[18] and also 2D materials, such as InSe,[6] black phosphorus,[11] and Bi_2O_2Se.[35] Our

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experiments show that multiplication factors induced from either electrons or holes in ambipolar 2D materials can be measured independently, and the measured relationship between $1 - 1/M$ and V_{ds} plotted for both electrons and holes of WSe_2 is provided in Figure 5a and b, respectively. Measurements at various gate voltages show no notable difference between the values of M and the slope of the graphs, which is anticipated because V_g influences only the total number of charge carriers involved in the carrier multiplication process but not the lateral field strength that drives the impact ionization in the 2D channel. The average values of the parameter n in electron- and hole-induced multiplication are determined to be ~8.82 and ~5.01, respectively, for the selected device. However, these values ranged between 3 and 9 in different devices. Such variance has been previously observed in Si bipolar junction transistors (BJTs) with values from 2 to 5 and is understood to be dependent on temperature and doping profile in the case of BJT structure.[36] In 2D FET systems, this variance could be affected by interfacial defects between the channel and the dielectric, which would hinder carrier multiplication due to increased scattering. Although additional experiments with the control of interfacial defects (*i.e.*, by using top and bottom hBN encapsulation) would lead to more reliable results, the values of parameter n observed in WSe_2 FETs are consistent within the range of reported values for other 2D semiconductors.[6,11,12]

The breakdown voltages V_b with respect to the channel length L of various devices are plotted in Figure 5c. The relationship clearly shows a linear dependence of V_b on L. The slope of the graphs ($V_b/L = E_b$) defines the breakdown field, which is an intrinsic property of the semiconductor material. The E_b values of electrons and holes deduced from our experiments are ~346 and 218 kV/cm, respectively, which are comparable to the previously reported values for MoS_2.[9]

Another important parameter describing the avalanche multiplication phenomenon in a semiconductor material is the impact ionization rate α, which is defined as the number of generated electron−hole pairs by an initial charge carrier per unit distance traveled.[37] The impact ionization rates can be approximately deduced from the multiplication factor M through the relationship[38] $\alpha = 1/L(1 - 1/M)$, under the assumption that the electric field in the channel is almost uniform (see Section 11 in the Supporting Information for a detailed discussion). The calculated α values for electrons and holes are plotted in Figure 5d along with reported values of various materials.[39,40] The impact ionization rate is naturally a function of electric field because the charge carriers can acquire enough kinetic energy to induce ionization at a shorter distance when the applied field is stronger. The model widely used in the literature to characterize impact ionization rates is the Shockley model,[41] given by $\alpha_{n,p} = \alpha^{\infty}_{n,p} \exp(-\beta_{n,p}/E)$, where the subscript n and p represent electrons and holes, respectively, and $\alpha^{\infty}_{n,p}$ and $\beta_{n,p}$ are the ionization coefficients. Our data measured from the representative WSe_2 FET are well fitted to the model, as shown by the fit lines (red lines) in Figure 5d, with $\alpha_n = 1.08 \times 10^7 \exp(-1.79 \times 10^6/E)$ and $\alpha_p = 1.31 \times 10^6 \exp(-1.08 \times 10^6/E)$. The values of α_n and α_p calculated from other devices are summarized in Section 12 in the Supporting Information.

The obtained ionization rates of WSe_2 can be explained from the band gap analysis in 3D materials. From the band-to-band ionization model discussed in Figure 4d, materials with a higher band gap require a higher electric field to initiate impact ionization, and the data from the previously reported bulk materials followed this trend as shown in Figure 5d. WSe_2, with a band gap (~1.2 eV) similar to Si (1.12 eV), has ionization rates close to Si in the evaluated range. Note that the β values (*i.e.*, the slope of the graphs in Figure 5d) of WSe_2 are found to be similar to those of conventional 3D materials. However, there has been little research that has explicitly evaluated the ionization rates of 2D materials to determine if there is a fundamental difference in ionization rates of 2D materials from those of 3D materials.

Another interesting feature is the relative magnitude of ionization rates of electrons and holes. The ionization rate of electrons in WSe_2 is lower than that of holes, similar to most 3D materials, whereas the opposite is true for Si. This result agrees with the breakdown fields obtained in Figure 5c, because electrons would require higher electric field to initiate avalanche breakdown due to their lower ionization rate than holes. A fundamental reason behind this discrepancy is not clearly understood, but combined effects of effective mass, mean free path, and also the shape of the bands near the band gap are expected to influence the ionization rates.[33,42] Further studies on impact ionization in other semiconductors are desired for understanding the precise physics determining the ionization rates of electrons and holes.

CONCLUSIONS

In conclusion, we characterized the ambipolar transport and avalanche multiplication phenomena in 2D WSe_2 FETs under high voltages through the channel length modulation. The two phenomena were differentiated by analyzing the secondary increase in output current and the dependence of critical (breakdown) voltages on the gate voltage. Ambipolar transport was achieved in devices with channel lengths exceeding ~1 μm through the inversion of effective gate voltage near the drain electrode and was identified by the linearly increasing critical voltage in accordance with gate voltage. On the other hand, avalanche multiplication was induced in short-channel devices by a high lateral electric field, with the multiplicative behavior showing little dependence on the applied gate voltage. We further investigated the impact ionization rates and breakdown voltages by electrons and holes separately. The observed differences in the multiplicative properties between electrons and holes call for further studies on the fundamental mechanism of field-induced carrier multiplication processes, especially in promising 2D materials for next-generation technology. Our work will enhance the understanding of the avalanche multiplication characteristics in atomically thin materials and contribute to the development of high-performance and emerging device architectures through selective integration of ambipolar transport and avalanche multiplication.

METHODS

Device Fabrication. Few-layer WSe_2 flakes were first transferred onto a 270 nm thick SiO_2/Si substrate from the bulk crystal by mechanical exfoliation to fabricate WSe_2 FETs. Then, on top of WSe_2 flakes, a double-electroresist layer of methyl methacrylate (9% concentration in ethyl lactate) and poly(methyl methacrylate) (950 000 molecular weight, 5% concentration in anisole) was spin-coated at 4000 rpm. Each resist layer was baked at 180 °C for 90 s on a hot plate after coating. The electron-beam lithography method (JSM-6610, JEOL) was used to pattern the source and drain electrodes, and Pd (50 nm thick) was deposited with an electron-beam evaporator system (KVE-2004L, Korea Vacuum Tech.) for the

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formation of electrodes. The fabricated WSe_2 FETs were annealed at 150 °C for 1 h for enhancement of electrical performance.

Optical and Electrical Characterization. Raman and PL spectra of WSe_2 crystals were measured using a 532 nm laser with an intensity of 30 μW as the excitation source (XperRam 200, Nanobase Inc.). FE-SEM images were taken using a JSM-7800F Prime (JEOL Ltd., Japan). Next, the thickness of WSe_2 flakes was measured using an atomic force microscope (AFM) (NX10, Park Systems). Finally, the electrical characteristics of the devices were measured using a semiconductor parameter analyzer (Keithley 4200-SCS) in a vacuum.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.1c08104.

Device fabrication process, parabolicity of long-channel device $I-V$ curves, band structure illustration on the effect of V_g on ambipolar transport, ambipolar transport of various devices, transfer curve and avalanche multiplication characteristics of short-channel devices, permanent Joule breakdown of WSe_2 FETs, avalanche multiplication in various devices, determination of breakdown voltage (V_b), device parameters of the long-channel devices, ambipolar transport mechanism starting from p-type, determination of α from the multiplication factor, values of α and β observed in various WSe_2 FETs, and PL spectra of WSe_2 flakes (PDF)

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Notes

The authors declare no competing financial interest.

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