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Towards flexible CMOS circuits

Tellurium thin films evaporated at cryogenic temperatures facilitate the realization of high performance wafer-scale flexible *p*-type field-effect transistors and various types of logic gates.

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Complementary metal oxide semiconductor (CMOS) technology has been at the core of applications in digital logic circuits, communication, signal sensing and memory chips[1,2]. CMOS is a type of metal–oxide–semiconductor field-effect transistor (MOSFET) technology that uses symmetrical pairs of p-type and n-type MOSFETs for logic functions. Specifically, its attractive advantages over unipolar transistors such as low static power consumption, high noise immunity and logic swing output have tremendously accelerated the growth of today's digital world[2]. However, for some applications such as wearable electronics, the technological demands towards physical flexibility and robustness of large-area electronic devices go beyond conventional silicon-based CMOS technology[1,3,4]. From the perspective of flexibility, the deposition of semiconductors must be performed at low temperatures maintaining their high electrical performance, energy efficiency and large-scale integration capability.

In the past few decades, various types of semiconductors and flexible substrates have been used to realize low-temperature processed field-effect transistors (FETs). In particular, amorphous metal-oxide n-type semiconductors[4], such as amorphous InGaZnO (a-IGZO), ZnO, IZO and InO_x deposited at plastic-compatible temperatures (<200 °C) or at room-temperature with the assistance of photochemical activation have shown suitable electrical performance for active-matrix electronics, including displays and sensor arrays[5]. Although low-temperature processed Cu_xO, NiO_x and SnO have emerged as p-type oxide-based materials[6], their intrinsically lower electrical performance including a hole mobility of ~1 $cm^2\ V^{-1}\ s^{-1}$ compared to that of n-type semiconductors is a critical bottleneck for realizing high performance and energy-efficient CMOS applications. The discovery of low-dimensional p-type semiconductors such as carbon nanotubes, nanowire-based materials and two-dimensional (2D) transition metal dichalcogenides, has ushered in a new class of alternative flexible p-type materials with tunable electrical properties[3,7]. However, as far as the use of low-dimensional materials is concerned, further improvements towards large-scale integration with high device yield are required. Although many research groups have been intensively working on high performance p-type organic semiconducting devices owing to low-temperature processing advantages[8], their potential applications are still limited due to intrinsically inferior electrical performance and environmental stability.

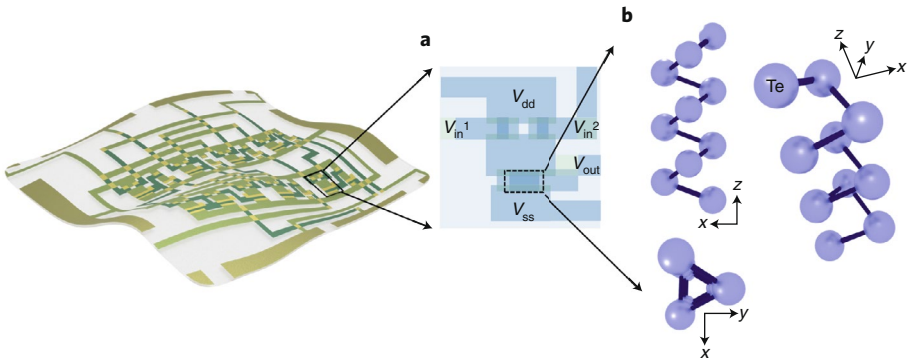

Fig. 1 | A schematic image showing a flexible computational circuit of 2-bit multiplier with 39 Te field-effect transistors. a, Top-view schematic image of a NAND gate based on a *p*-MOS inverter. For the MOS fabrication, Ti/Au (2 nm/18 nm) gate electrodes were deposited by e-beam evaporation. On the gate electrodes, the ZrO_2 dielectric layer was deposited by atomic layer deposition. For the channel layer, 8 nm-thick Te thin films were deposited onto a −80 °C substrate, and then 30 nm-thick Ni electrodes were deposited by e-beam evaporation as metal contacts. Javey and co-workers[9] showed feasibility to realize high performance *p*-MOS by conventional evaporation systems in plastic-compatible temperatures. Here, V_{in}, V_{out}, V_{dd}, and V_{ss} are the input voltage, output voltage, positive supply voltage and negative supply voltage (or ground), respectively. **b**, Perspective, top and side views of the crystal structure of Te, which is composed of covalently-bonded atoms in a helical chain along a single axis.

Writing in *Nature Nanotechnology*, Javey and co-workers have reported tellurium thin films obtained via thermal evaporation at cryogenic temperatures that can facilitate the realization of high performance wafer-scale flexible p-type FETs and various types of logic[9].

Previous reports have already demonstrated that single-crystalline Te nanostructures exhibit excellent hole mobility of a few hundred $cm^2\ V^{-1}\ s^{-1}$ (ref. [10]), however the realization of Te-based large-area FETs at plastic-compatible temperatures remains challenging. Specifically, because the domain size of Te films largely determines their electrical performance including hole mobility, further optimization of the Te film growth conditions is required. To address this issue, thermal evaporation at cryogenic temperatures was employed to improve the Te film quality, especially for achieving larger domains. The authors have also systematically investigated the effects of the evaporation temperature on the domain size and the electrical performance. As a result, FETs based on Te films evaporated at a substrate temperature of −80 °C exhibit an effective hole mobility of ~35 $cm^2\ V^{-1}\ s^{-1}$, an on/off ratio of ~10^4 and a subthreshold swing of 108 mV dec^{-1} measured at room temperature. This desirable p-type behaviour is primarily attributed to an increased domain size, which was not observed for Te films deposited at higher temperatures. Interestingly, the effective hole mobilities extracted for the temperature range 77–300 K show no temperature dependence indicating that this parameter is critically limited by the

grain boundary in the Te films. Therefore, the reported p-type Te films together with the mature low-temperature processed n-type semiconductors may offer a potential solution for realizing high performance large area flexible CMOS platforms. To illustrate the potential of the presented concept, Javey and co-workers show the realization of various flexible logic gates and computational circuits, such as an inverter, NAND gate (Fig. 1), full adder and multiplier composed of dozens of transistors through conventional semiconductor processing[9]. These demonstrations were not possible with other emerging p-type candidates. Furthermore, the authors construct monolithic three-dimensional (3D) integrated circuits and back-end-of-line electronics achieving high density integration.

In the future, more feasible strategies enabling the realization of improved flexible complementary ICs will be needed for even higher integration density, better device-to-device uniformity, high operating speed and low power consumption. Currently, the deposition of Te, which takes place at −80 °C, is not industrially compatible. However, this work clearly indicates that the approach of employing thermally evaporated Te films is beneficial in terms of providing sufficient electrical performance to match the available n-type semiconductors. In addition, existing facilities for fabricating conventional silicon-based electronics can be utilized with high reliability in batch manufacturing, which allows the realization of complex computational circuits and monolithic 3D integrated circuits based on CMOS technology with minimized additional costs. For tellurium, to qualify as a promising p-type material, further studies should focus on ensuring higher quality (for example, crystallinity, domain size and impurities) of thermally evaporated Te thin films and better CMOS compatibility of the deposition process (for example, substrate temperature). If these requirements can be met, this approach could accelerate the coming of the Internet of Things world connected by energy-efficient flexible 3D electronics. ❐

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