The Effect of Nanoscale Nonuniformity of Oxygen Vacancy on Electrical and Reliability Characteristics of HfO_2 MOSFET Devices

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***Abstract*—To understand the influence of oxygen vacancies in HfO_2 on the electrical and reliability characteristics, we have investigated area-dependent leakage-current characteristics of HfO_2 with large-area device and conducting atomic force microscopy (C-AFM). Unlike with the large-area analysis with typical capacitor and transistor, a clear evidence of oxygen vacancy was observed in nanoscale-area measurement using the C-AFM. Similar observations were made in various postdeposition annealing ambients to investigate the generation and reduction of oxygen vacancy in HfO_2. With optimized postdeposition annealing for oxygen vacancy, significantly reduced charge trapping was observed in HfO_2 nMOSFET.**

***Index Terms*—Charge trapping, conducting atomic force microscopy (C-AFM), hafnium oxide, oxygen vacancy.**

I. Introduction

HIGH-κ GATE dielectrics have been investigated to replace silicon dioxide (SiO_2) as the gate dielectric for future CMOS technologies [1]–[3]. Among the high-κ dielectrics, the Hf-based dielectrics are intensively studied due to their compatibility with the conventional CMOS process [3]–[5]. However, to implement Hf-based dielectric into conventional CMOS process, threshold voltage $(V_{\rm th})$ instability and reliability degradation issues caused by charge trapping should be solved [6]–[8]. When physical thickness of high-κ dielectric is decreased, a significant improvement of device performance was observed, owing to the reduction of charge-trap site [9]. But, without clear understanding on charge-trapping mechanism, a high-performance transistor with good reliability may not be achieved.

Recently, either by physical analysis or atomic simulation, oxygen vacancy was proposed to explain the origin of charge trapping in high-κ dielectric [10]–[12]. Due to the analysis difficulty of nanoscale behavior with capacitor and transistor, oxygen-vacancy generation and passivation during the fabrication process have not been clearly understood. For that reason, C-AFM was used to understand the nanoscale behavior of HfO_2 [13], [14]. However, a systematic nanoscale analysis of HfO_2 depending on postdeposition annealing (PDA) has not been carried out. In this letter, we will investigate the electrical characteristics of HfO_2 in nanosize area with C-AFM measurement and correlate this result with oxygen vacancy.

II. Experiments

After standard cleaning of 200-mm n-type silicon wafer, SiO_x interfacial layer was formed with an ozone oxidizing method. A 3-nm-thick HfO_2 was deposited by atomic-layer-deposition method. Then, PDA was performed at 700 °C for 1 min in various ambients (NH_3, N_2, and O_2). To observe the electrical characteristics depending on PDA, Pt/HfO_2 capacitor and TiN/HfO_2 MOSFET were fabricated by using the conventional CMOS process. To fabricate HfO_2 MOSFET with minimal interfacial layer regrowth and boron diffusion into a dielectric, one set of MOSET samples was performed with PDA in NH_3 ambient. To understand the charge-trapping effect depending on the PDA, another set of MOSFET samples was performed with an additional O_2 PDA after the NH_3 PDA. Finally, forming gas annealing $(H_2/N_2 = 3\%/97\%)$ was performed at 400 °C for 30 min in atmospheric ambient.

For nanoscale-area analysis of HfO_2, a C-AFM measurement in atmospheric ambient was employed. A Pt-coated Si cantilever was used as a nanosize tip. The size of the C-AFM tip is around 300 nm^2. To measure the wide range of leakage current, a source and measure unit in Agilent 4155 was connected to the AFM system. To avoid the damage of the tip from ionic contamination during measurement, electrons were injected from the substrate [15].

III. Results and Discussion

Gate leakage-current density (J_g) (at $V_g - V_{\rm fb} = 1$ V) and capacitance–voltage characteristics of 3-nm HfO_2 depending on PDA are shown in Fig. 1. Due to the uniform depositions of HfO_2 film, all measured spots showed uniform distribution of J_g. The reduction of J_g and the increase of equivalent oxide thickness (EOT) was observed in N_2 and O_2 PDA samples (around 0.2 nm) and can be explained by interfacial-layer regrowth during the PDA process.

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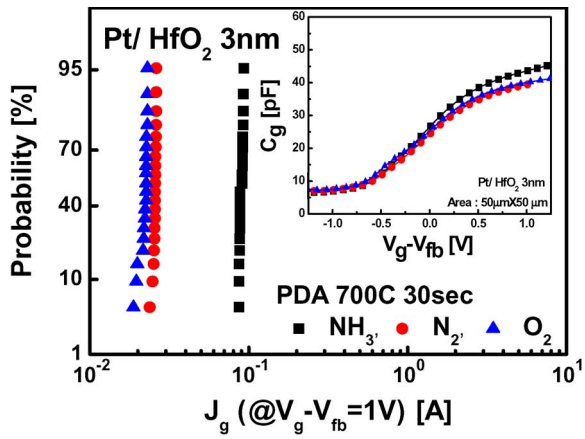

Fig. 1. Gate leakage-current density and capacitance–voltage characteristics of 3-nm HfO_2 depending on PDA. Gate leakage current of each sample was extracted at $V_g - V_{\rm fb} = 1$ V, and measured area is 2.5×10^{-5} cm^2.

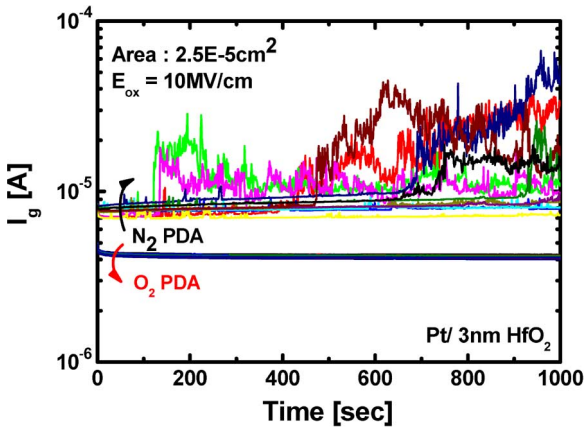

Fig. 2. Charge-trapping characteristics depending on N_2 and O_2 PDA. To maximize the charge trapping in HfO_2 layer, 10 MV/cm of electrical field $(V_g - V_{\rm fb}/{\rm EOT})$ stress was applied to the gate. At this field, electrons are injected through the triangular region of HfO_2 conduction band. To generalize the results, 12 different spots were measured for the same PDA condition.

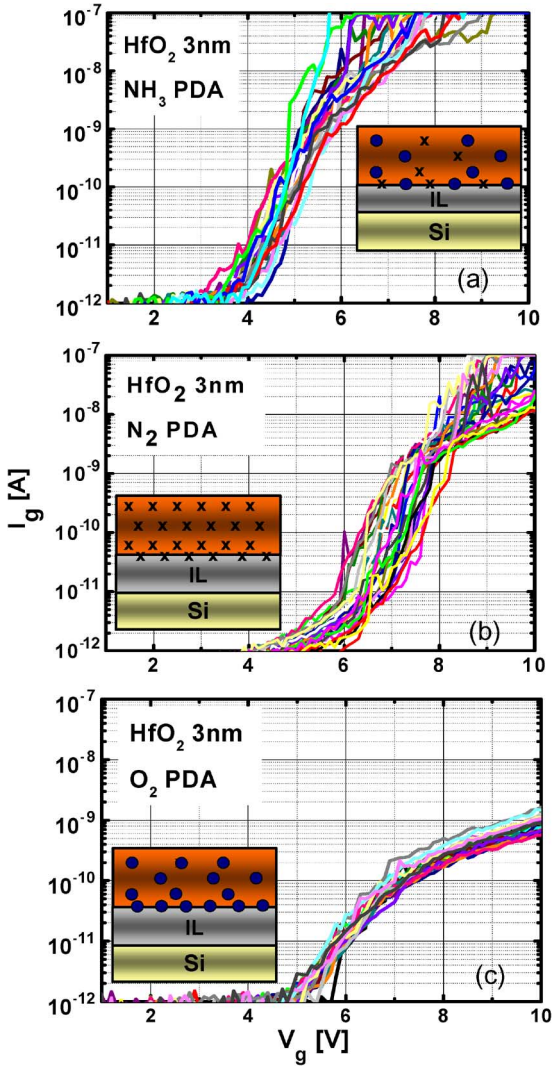

Fig. 3. I–V characteristics of 3-nm HfO_2 in nanoscale area depending on PDA. PDA was performed at 700 °C for 1 min in (a) NH_3, (b) N_2, and (c) O_2 ambients. Inset represents the generation and passivation of oxygen vacancy depending on PDA.

To investigate the charge-trapping behavior depending on PDA, 10 MV/cm of constant field stress was applied to N_2 and O_2 PDA samples (Fig. 2). At this field, electrons are injected through the triangular region of HfO_2 conduction band, and charge trapping in HfO_2 layer can be maximized. The oxygen PDA sample showed a minimal charge trapping, whereas the sample with N_2 PDA showed a significant charge trapping and a soft breakdown during stress. Considering a similar accumulation capacitance after PDA, the increased charge trapping and soft breakdown in N_2 PDA might be explained by the increased charge-trap site in HfO_2.

To clearly understand the dielectric property of HfO_2 depending on PDA, electrical characteristics in nanoscale regime were evaluated with C-AFM. Before nanoscale analysis of HfO_2, 3-nm-thick SiO_2 was measured as a control (data not shown here). C-AFM measurement with SiO_2 showed a uniform current flow and breakdown field regardless of the measured spot and area, suggesting that the distribution of traps in SiO_2 is quite uniform. This uniform gate leakage current in SiO_2 also suggests that measurement error induced by surface contamination is negligible. On the other hand, the current–voltage $(I$–$V)$ characteristics of HfO_2 in nanoscale-area were somewhat different from that of SiO_2. Fig. 3 shows the I–V characteristics of HfO_2 depending on PDA. A wide distribution of gate leakage current (I_g) was observed in HfO_2 with N_2 PDA. Compared with N_2 PDA, NH_3 PDA showed the reduction of I_g variation in low-voltage region (4–6 V). Considering the band bending of dielectric and the I–V characteristics together, nitrogen incorporation is effective for the trap passivation in HfO_2 layer and reduces I_g variation. The weak improvement of I_g in high-voltage region ($>$ 6 V) can be understood by the reliability characteristics of thin SiO_x interfacial layer [13]. However, even if nitrogen incorporation into HfO_2 helps the reduction of I_g, HfO_2 still showed the large variation of I_g. This result indicates that the origin of nanoscale nonuniformity of I_g in HfO_2 cannot be fully cured with nitrogen. Compared with NH_3 and N_2 PDA, the sample with O_2 PDA showed a significant reduction of I_g variation. Considering a similar EOT with N_2 PDA, the significant reduction of I_g

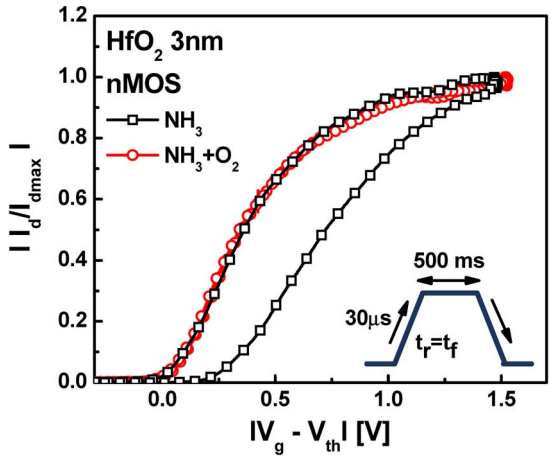

Fig. 4. Single pulsed I_d–V_g characteristics of 3-nm HfO_2 nMOSFET. Compared with NH_3 PDA, O_2 PDA followed by NH_3 PDA showed a significant reduction of charge trapping during measurement.

variation after O_2 PDA could not be explained with interfacial-layer regrowth. The reduction of I_g variation after O_2 PDA can be explained by the successful passivation of oxygen-vacancy-related traps in HfO_2 [10]. Based on these findings, the nanoscale nonuniformity of I_g in HfO_2 should be explained by oxygen vacancy and can be cured with oxygen treatment.

The I_g variation in the nanoscale area can be understood with the inset of Fig. 3. During NH_3 and O_2 PDA, nitrogen and oxygen incorporated into HfO_2 dielectric and passivated trap sites. However, during N_2 PDA, only oxygen migration occurred due to the inert property of N_2 gas. Thus, a wide variation of I_g was observed in N_2 PDA because of the increased oxygen-vacancy site in the HfO_2 layer.

The effects of oxygen-vacancy passivation on charge trapping and reliability were evaluated by single pulsed I_d–V_g measurement (Fig. 4). Compared with NH_3 PDA, O_2 PDA followed by NH_3 PDA showed a significant reduction of hysteresis. The significant reduction of hysteresis also suggests the effective passivation of oxygen vacancy in HfO_2 layer.

IV. Summary

The charge-trapping characteristics of the HfO_2 and the effect of oxygen-vacancy site are clearly correlated with large and nanoscale-area analyses. C-AFM study of HfO_2 in nanoscale-area showed that the nanoscale nonuniformity of gate leakage current is strongly dependent on the PDA conditions. The significant reduction of gate leakage-current nonuniformity after oxygen annealing indicates that the oxygen vacancy can be a major source of gate leakage current and origin of charge-trap sites in HfO_2. To a achieve high-performance HfO_2 transistor with good reliability, a careful optimization of dielectric properties to minimize oxygen vacancies is necessary.

References

[1] E. P. Gusev, A. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha, A. Callegari, S. Zafar, P. C. Jamison, D. A. Neumayer, M. Copel, M. A. Gribelyuk, H. Okorn-Schmidt, C. D'Emic, P. Kozlowski, K. Chan, N. Bojarczuk, L.-A. Ragnarsson, P. Ronsheim, K. Rim, R. J. Fleming, A. Mocuta, and A. Ajmera, "Ultrathin high-κ gate stacks for advanced CMOS devices," in *IEDM Tech. Dig.*, 2001, pp. 451–454.

[2] J. C. Lee, H. J. Cho, C. S. Kang, S. Rhee, Y. H. Kim, R. Choi, C. Y. Kang, C. Choi, and M. Abkar, "High-κ dielectrics and MOSFET characteristics," in *IEDM Tech. Dig.*, 2003, pp. 95–98.

[3] T. Iwamoto, T. Ogura, M. Terai, H. Watanabe, H. Watanabe, N. Ikarashi, M. Miyamura, T. Tatsumi, M. Saitoh, A. Morioka, K. Watanabe, Y. Saito, Y. Yabe, T. Ikarashi, K. Masuzaki, Y. Mochizuki, and T. Mogami, "A highly manufacturable low power and high speed HfSiO CMOS FET with dual poly-Si gate electrodes," in *IEDM Tech. Dig.*, 2003, pp. 639–642.

[4] S.-C. Song, Z. Zhang, C. Huffman, J. H. Sim, S. H. Bae, P. D. Kirsch, P. Majhi, R. Choi, N. Moumen, and B. H. Lee, "Highly manufacturable advanced gate-stack technology for sub-45-nm self-aligned gate-first CMOSFETs," *IEEE Trans. Electron Device*, vol. 53, no. 5, pp. 979–989, May 2006.

[5] H.-S. Jung, J.-H. Lee, S. K. Han, Y.-S. Kim, H. J. Lim, M. J. Kim, S. J. Doh, M. Y. Yu, N.-I. Lee, H.-L. Lee, T.-S. Jeon, H.-J. Cho, S. B. Kang, S. Y. Kim, I. S. Park, D. Kim, H. S. Baik, and Y. S. Chung, "A highly manufacturable MIPS (metal inserted poly-Si stack) technology with novel threshold voltage control," in *VLSI Symp. Tech. Dig.*, 2005, pp. 232–233.

[6] B. H. Lee, C. D. Young, R. Choi, J. H. Sim, G. Bersuker, C. Y. Kang, R. Harris, G. A. Brown, K. Matthews, S. C. Song, N. Moumen, J. Barnett, P. Lysaght, K. S. Choi, H. C. Wen, C. Huffman, H. Alshareef, P. Majhi, S. Gopalan, J. Peterson, P. Kirsh, H.-J. Li, J. Gutt, M. Gardner, H. R. Huff, P. Zeizoff, R. Murto, L. Larson, and C. Ramiller, "Intrinsic characteristics of fast transient charging effects (FCTE)," in *IEDM Tech. Dig.*, 2004, pp. 859–862.

[7] S. Zafar, A. Kumar, E. Gusev, and E. Cartier, "Threshold voltage instabilities in high-κ gate dielectric stacks," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 1, pp. 45–64, Mar. 2005.

[8] H. Park, R. Choi, B. H. Lee, S.-C. Song, M. Chang, C. D. Young, G. Bersuker, J. C. Lee, and H. Hwang, "Decoupling of cold-carrier effects in hot-carrier reliability assessment of HfO_2 gated nMOSFETs," *IEEE Electron Device Lett.*, vol. 27, no. 8, pp. 662–664, Aug. 2006.

[9] P. D. Kirsch, S. C. Song, J. H. Sim, S. Krishnan, J. Gutt, J. Peterson, H.-J Li, M. Quevedo-Lopez, C. D. Young, R. Choi, J. Barnett, N. Moumen, K. S. Choi, C. Huffman, P. Majhi, M. Gardner, G. Brown, G. Bersuker, and B. H. Lee, "Mobility enhancement of ALD HfO_2/TiN gate stacks through improved charge trapping characteristics of 2.0 nm HfO_2," in *Proc. ESSDERC*, 2005, pp. 367–370.

[10] H. Takeuchi, D. Ha, and T.-J. King, "Observation of bulk HfO_2 defects by spectroscopic ellipsometry," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 22, no. 4, pp. 1337–1341, Jul. 2004.

[11] K. Torii, H. Kitajima, T. Arikado, K. Shiraishi, S. Miyazaki, K. Yamabe, M. Boero, T. Chikyow, and K. Yamada, "Physical model of BTI, TDDB and SILC in HfO_2-based high-κ gate dielectrics," in *IEDM Tech. Dig.*, 2004, pp. 859–862.

[12] Y. P. Feng, A. T. L. Lim, and M. F. Li, "Negative-U property of oxygen vacancy in cubic HfO_2," *Appl. Phys. Lett.*, vol. 87, no. 6, p. 062 105, Aug. 2005.

[13] L. Aguilera, M. Porti, M. Nafria, and X. Aymerich, "Charge trapping and degradation of HfO_2/SiO_2 MOS gate stacks observed with enhanced CAFM," *IEEE Electron Device Lett.*, vol. 27, no. 3, pp. 157–159, Mar. 2006.

[14] K. Kyuno, K. Kita, and A. Toriumi, "Evolution of leakage paths in HfO_2/SiO_2 stacked gate dielectrics: A stable direct observation by ultrahigh vacuum conducting atomic force microscopy," *Appl. Phys. Lett.*, vol. 86, no. 6, p. 063 510, Feb. 2005.

[15] M. Porti, M. Nafría, X. Aymerich, A. Olbrich, and B. Ebersberger, "Electrical characterization of stressed and broken down SiO_2 films at a nanometer scale using a conductive atomic force microscope," *J. Appl. Phys.*, vol. 91, no. 4, pp. 2071–2079, Feb. 2002.