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Memory characteristics of a self-assembled monolayer of Pt nanoparticles as a charge trapping layer

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Abstract

A self-assembled monolayer of Pt nanoparticles (NPs) was studied as a charge trapping layer for non-volatile memory (NVM) applications. Pt NPs with a narrow size distribution (diameter ~4 nm) were synthesized via an alcohol reduction method. The monolayer of these Pt NPs was immobilized on a SiO_2 substrate using poly(4-vinylpyridine) (P4VP) as a surface modifier. A metal-oxide-semiconductor (MOS) type memory device with Pt NPs exhibits a relatively large memory window of 5.8 V under ±7 V for program/erase voltage. These results indicate that the self-assembled Pt NPs can be utilized for NVM devices.

1. Introduction

Nanocrystal floating gate memory devices have attracted attention as one of the strong candidates for non-volatile memory (NVM) devices due to its scalability, electrical isolation and low charge leakage through the tunneling oxide [1, 2]. In particular, metal nanocrystals (NCs) have a number of advantages, such as higher density of states, large work function and strong charge confinement, which allow NVM devices to operate with low power, better retention and high density [3]. Various methods have been employed to form uniform metal NCs, including e-beam evaporation, molecular beam epitaxial and oxide reduction [3–5]. However, most of these methods require high temperature annealing for the formation of metal NCs, which results in metallic contamination, formation of metal compounds, and NCs with non-uniform size and arbitrary shape [5, 6]. Therefore, fabrication of memory devices using synthesized metal nanoparticles (NPs) has been investigated to overcome these drawbacks [7–10]. Various methods, such as colloidal suspension, spin coating, evaporation and biomolecule templates, have been applied to fabricate the monolayer of NPs [8–12]. Although such methods have showed relatively good results for the formation of a monolayer, difficulties remain with forming a monolayer of NPs on a certain substrate without aggregations. In addition, removing the chemical residue that results as a by-product of the chemical synthesis of metal NPs and using chemicals to transfer NPs onto a substrate pose challenging difficulties. It was shown that the chemical residue significantly degrades the electrical property of metal-oxide-semiconductor (MOS) devices [13]. Therefore, a new method should be developed to produce a highly uniform monolayer of NPs on a substrate without the chemical residue.

Recently, Kwon *et al* used an organic surfactant as an efficient adhesive for the immobilization of ferritin nanoparticles, because this molecule provides many binding sites for simultaneous interaction with both particles and a substrate, and it is easily removed via a comparably low temperature heat treatment [11]. Similarly, poly(4-vinylpyridine) (P4VP), which has a pyridyl group, provides strong adhesion to the surface and nanoparticles and is easily decomposed via heat treatment [14, 15]. These properties of P4VP are appropriate for the formation of highly uniform self-assembled metal NPs on a substrate and for the fabrication of MOS devices.

In this study, we synthesized platinum (Pt) NPs and fabricated a self-assembled monolayer (SAM) on a thermally grown SiO_2 substrate. For the immobilization of a Pt NP monolayer with a high dot density, P4VP as a surface modifier was employed. In addition, the electrical characterization of Pt NPs monolayer as a charge trapping layer in NVM was also investigated.

2. Experimental details

2.1. Formation of the Pt NP monolayer

Pt NPs were synthesized by modifying a simple method to control the size of Pt NPs with the use of an alcohol reduction, following the method in [15].

To prepare the self-assembled Pt NP monolayer, a p-Si substrate with a 3.7 nm thick silicon oxide was cleaned for 10 min in piranha solution followed by oxygen plasma treatment for a uniform hydrophilic surface. The substrate was dipped in a surface modifier, 1 wt% poly(4-vinylpyridine) (P4VP, $M_w = 160\,000$) solution in reagent alcohol (HPLC) [14]. After washing the polymer with fresh alcohol to remove excess polymer, the substrate was baked in an oven at 120 °C for 2 h. Subsequently, the substrate was dipped in a solution containing synthesized Pt particles for 3 min while stirring and then immediately put in a clean container to control the evaporation ratio. By carefully controlling the evaporation rate of the solvent, an almost uniform monolayer of Pt NPs was obtained. Field emission scanning electron microscopy (FE-SEM, Hitachi S-4700) and high resolution transmission electron microscopy (HR-TEM, Tecnai F20) were performed to analyze the size and distribution of Pt NPs.

2.2. Electrical characterization of the Pt NP monolayer

An MOS capacitor memory device employing a self-assembled Pt NP monolayer as a charge trap layer was fabricated. Self-assembled Pt NPs with and without a surface modifier were prepared for comparison in this study. For both samples, the removal of the immobilization agent was performed by heat treatment at 200 °C for 1 h in an Ar environment to remove P4VP and all chemical residues and to minimize the aggregation of Pt NPs. A 13 nm thick $LaAlO_3$ layer was deposited on the SiO_2/Pt-NPs via an e-beam evaporator. Subsequently, a 100 nm thick Pt gate electrode was deposited and patterned by photolithography. Standard post-metallization annealing in a forming gas (H_2:N_2 = 3:97) was performed at 400 °C for 30 min. For the control samples, a Pt-$LaAlO_3$/SiO_2/Si stack capacitor without Pt NPs and surface modifier was also fabricated. To analyze the bonding of Pt and the chemical residue, x-ray photoelectron spectroscopy (XPS) was performed. Using an HP 4284 LCR meter and an HP4155C semiconductor parameter analyzer, high frequency capacitance–voltage (C–V) measurements demonstrated the device operating as a memory device.

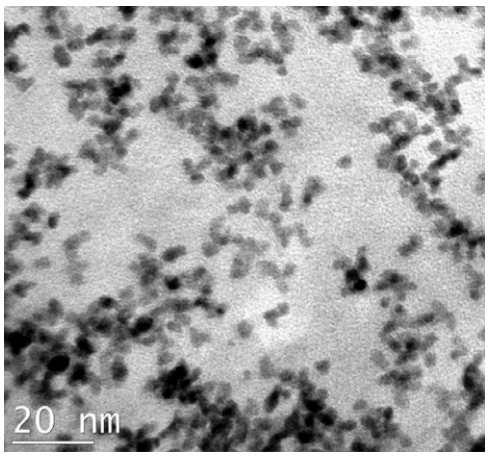

Figure 1. TEM image of Pt nanoparticles prepared on a carbon-coated copper grid. A drop of the Pt colloidal solution was deposited on a copper grid and the image was acquired.

3. Results and discussion

Figure 1 shows an HR-TEM image of synthesized Pt NPs produced by the alcohol reduction methods. A drop of Pt colloidal solution was deposited on a carbon-coated copper grid and the image was acquired. Although nanoparticles do not possess a well-ordered and close-packed arrangement, crystalline Pt NPs with a narrow size distribution were observed. Average particle diameter was around 4 nm.

For the immobilization of a Pt NP monolayer with a high dot density, P4VP as a surface modifier was employed. According to Malynych *et al*, a surface modifier, P4VP, is a universal monofunctional surface modifier, that is, only one type of functionality (pyridyl group) is required for the adhesion to surfaces and the binding of nanoparticles [14], because the pyridyl group has a strong affinity to metals and is able to undergo hydrogen bonding with polar species [14]. When the substrate is dipped in 1 wt% P4VP solution in alcohol, the surface is terminated with protonated silanol groups that form a hydrogen bond with the nitrogen atom on the pyridyl [14]. After the adsorption, P4VP molecules still have numerous unbound pyridyl groups that do not participate in the interaction with the surface and that are capable of binding of nanoparticles [14]. Therefore, a P4VP-coated substrate can immobilize the Pt NPs as a monolayer.

To confirm the monolayer formation of Pt NPs, SEM was performed. After heat treatment, the substrate having NPs without any chemical residues from the self-assembly procedure was observed. The self-assembled Pt NPs on SiO_2 with and without surface modifier are shown in figure 2. The self-assembled Pt NPs without surface modifier show aggregation and irregular distribution of NPs in figures 2(a) and (b) under different magnifications. On the other hand, utilizing a surface modifier, P4VP, the uniform distribution of Pt NPs without aggregation over a large area was obtained, as shown in figures 2(c) and (d). Dot density was estimated at approximately 6×10^{11} cm^{-2}, indicating successful self-assembly using the surface modifier for a monolayer of Pt NPs.

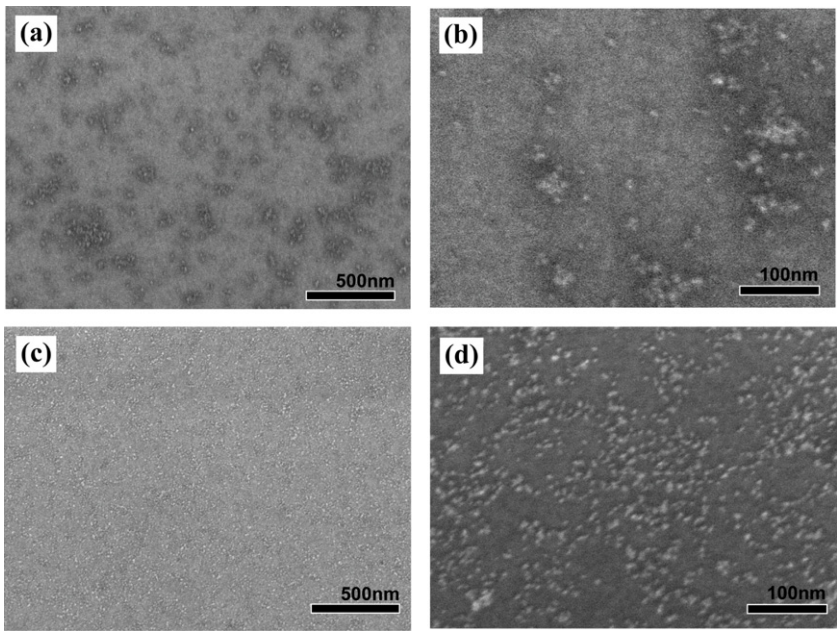

Figure 2. (a) SEM image of Pt nanoparticles after heat treatment, (b) without surface modifier, poly(4-vinylpyridine), and (c), (d) with surface modifier under different magnifications.

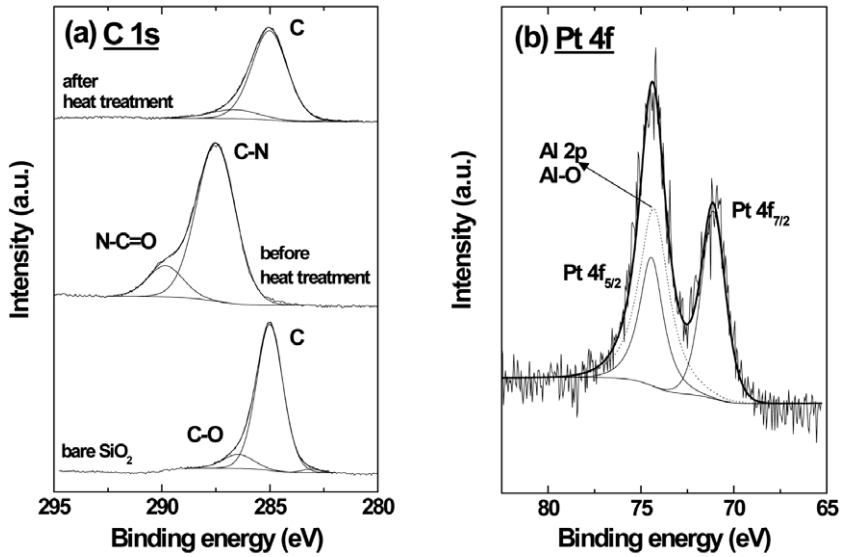

Figure 3. (a) XPS spectra of the bare SiO_2, self-assembled monolayer of Pt NP surfaces before and after heat treatment for the removal of the immobilization agent in the C 1s peak region. (b) The Pt 4f region of Pt NPs in the metal-oxide-semiconductor device stack.

Prior to fabrication of an MOS device, we evaluated the chemical residue after heat treatment. For the self-assembled monolayer of Pt NPs, P4VP was used. In the MOS device, this kind of chemical residue results in degraded electrical properties. The P4VP monolayer thickness is about 2 nm and the electron transfer rate decreases rapidly with the distance from the electrode by a factor of 2.718 for every 1.5 Å [16]. Therefore, the removal of chemical residue is important. To confirm the presence or absence of chemical residue, XPS analysis was performed. Figure 3(a) shows the XPS core-level spectra of the C 1s for the bare SiO_2 sample and SAM Pt samples with and without heat treatment. For the bare SiO_2 sample, a peak signal of carbon at 285 eV, a characteristic of carbon with no polymeric carbon contamination due to air exposure, was observed [17]. The weak signal of oxygen is believed to be a contamination due to exposure of the sample to air prior to the XPS analysis [18]. In the SAM of the Pt NP sample before heat treatment, the peak signals of C–N and N–C=O bonding were observed at 287.5 and 289.85 eV, respectively [12]. These peaks are from P4VP and indicate that with XPS the polymer can be differentiated from other peaks. However, the sample after heat treatment shows no polymeric carbon peaks. The peak signals for carbon and C–O bonding were only detected at the binding

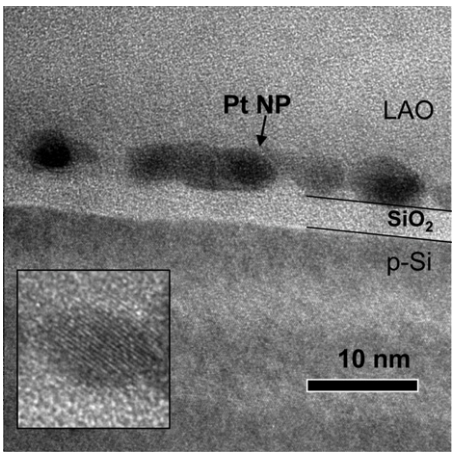

Figure 4. Cross-sectional HR-TEM image of a metal-oxide-semiconductor device structure containing a self-assembled monolayer of Pt NPs.

energy of C 1s. In addition, the N 1s spectra of P4VP also exhibit a symmetric peak at a binding energy of 399.25 eV for the sample before heat treatment (data not shown). This peak disappeared for the annealed sample. Based on these results, it can be concluded that the polymer used for the immobilization of NPs was completely removed after heat treatment. The chemical composition of Pt NPs after the fabrication of the MOS capacitor was checked by using the XPS spectra of Pt 4f, as shown in figure 3(b). The Ar sputtering was used in an XPS chamber to remove the $LaAlO_3$. The peaks for the binding energy of Pt $4f_{7/2}$ and Pt $4f_{5/2}$ were 71 and 74.3 eV, respectively, indicating the characteristic pure Pt metallic property [17]. Due to the blocking oxide ($LaAlO_3$), the peak signal of Al–O bonding was detected at 74.2 eV. In the stack, no carbon peak was detected. These results suggest that the metallic Pt NPs embedded in the MOS capacitor are well fabricated without any chemical residues.

Figure 4 shows a cross-sectional HR-TEM image of the MOS device containing self-assembled Pt NPs indicating a well-formed monolayer of crystalline Pt NPs with an average diameter of 4 nm. Thus, this technique has proven to be useful in minimizing particle aggregation and in making one monolayer of Pt NPs on substrates.

C–V hysteresis curves of the MOS memory device containing the SAM of Pt NPs are shown in figure 5(a). A sweep rate of 0.05 V s^{-1} and a holding time of 1 s were sufficient for the charging and discharging of the nanocrystal memory. Counterclockwise *C–V* hysteresis curves with large widths were obtained, indicating electron injection from the substrate to the charge trapping layer. The initial flatband voltage (V_{FB}) of the device without Pt NPs was approximately 0 V. The device without Pt NCs shows a negligible memory window at 7/−7V for its program/erase (P/E) voltage. On the other hand, SAM of Pt NP memory being utilized with a surface modifier shows a large memory window of 5.8V at the same P/E voltage. The Pt NP memory without a surface modifier shows a smaller memory window of 2.4 V mainly due to the aggregation and lower dot density. The slope of the *C–V* curves for the device without a surface modifier was degraded, indicating that the device has more interface states compared to the control sample. From this analysis of the device without a surface modifier, it can be suggested that the chemical residue was not removed completely due to the aggregation of NPs, thus having some incorporated interactions with interface trap states.

The charge storage effect of Pt NPs was characterized. Figure 5(b) shows the flatband voltages for different voltage sweeps. As program/erase voltages were increased, memory windows were also increased and then saturated. Maximum memory windows for the devices with and without a surface modifier were approximately 7 V and 2.8 V, respectively. The amount of charge stored in the Pt NPs can be estimated by the relation $Q = C\Delta V_{FB}$, where C is the capacitance density. In this work, C is about 3.4×10^{-7} F cm^{-2} for both samples. Thus, the electron densities stored in the Pt NPs with and without a surface modifier were estimated to be 15×10^{12} and 6×10^{12} cm^{-2}, respectively. The larger stored charge than the dot density can be explained by the multiple electron storage in Pt NPs [19].

Figure 6 shows the charge loss rate at 85 °C for the Pt NP-embedded MOS capacitor. V_{FB} was measured after program/erase of 5V/−5V. The Pt NP device shows good retention characteristics up to 10^4 s. This can be explained

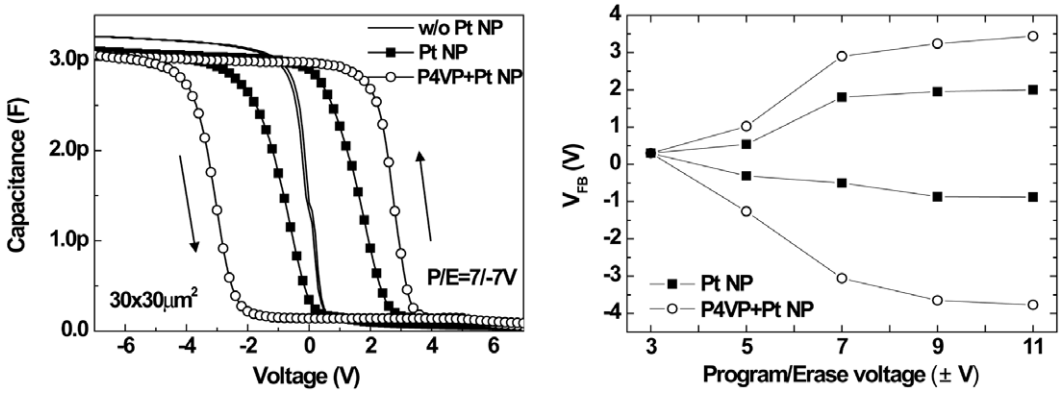

Figure 5. (a) High frequency *C–V* hysteresis of Pt nanocrystal memory utilized with and without a P4VP layer for a 50 μm × 50 μm area. (b) The flatband voltages for different voltage sweeps.

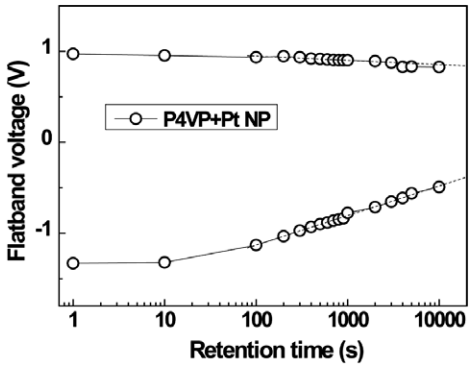

Figure 6. Charge loss characteristics of self-assembled monolayer of Pt NPs embedded in a MOS capacitor at 85 °C. The Pt NP device shows good retention characteristics up to 10^4 s.

by the deepest potential well of Pt NPs and by less metal contamination during the fabrication procedures [20].

4. Conclusion

A self-assembled monolayer of Pt NPs utilizing a surface modifier, P4VP, resulted in improved distribution of a Pt NC monolayer with a mean size of 4 nm and a dot density of 6×10^{11} cm^{-2} on the thermal oxide. Self-assembled Pt NPs were confirmed by SEM and TEM. The MOS capacitor memory with Pt NPs as the charge trapping layer showed a large memory window of 5.8 V under $+7/-7$ V for program/erase voltage as well as good retention. These results indicate that the self-assembled Pt NPs can be utilized for NVM devices.

Acknowledgments

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References

[1] Tiwari S, Rana F, Hanafi H, Hartstein A, Crabbé E F and Chan K 1996 *Appl. Phys. Lett.* **68** 1377
[2] Kobayashi T, Endoh T, Fukuda H, Nomura S, Sakai A and Ueda Y 1997 *Appl. Phys. Lett.* **71** 1195
[3] Lee C, Meteer J, Narayanan V and Kan E C 2005 *J. Electron. Mater.* **34** 1
[4] Sargentis C, Giannakopoulos K, Travlos A and Tsamakis D 2007 *Surf. Sci.* **601** 2859
[5] Tseng J-Y, Cheng C-W, Wang S-Y, Wu T-B, Hsieh K-Y and Liu R 2004 *Appl. Phys. Lett.* **85** 2595
[6] Kato H, Shibata Y and Kuwano H 1987 *Electron. Commun. Japan* 2 **70** 65
[7] Lee J-S, Cho J, Lee C, Kim I, Park J, Kim Y-M, Shin H, Lee J and Caruso F 2007 *Nat. Nanotechnol.* **2** 790
[8] Park B, Cho K, Kim H and Kim S 2006 *Semicond. Sci. Technol.* **21** 975
[9] Seol K S, Cho K S, Kim B-K, Choi J-Y, Lee E-K, Min Y-S, Park J-B and Choi S-H 2007 *J. Korean Phys. Soc.* **50** 49
[10] Paul S, Pearson C, Molloy A, Cousins M A, Green M, Kolliopoulou S, Dimitrakis P, Normand P, Tsoukalas D and Petty M C 2003 *Nano Lett.* **3** 533
[11] Kwon M, Choi H, Chang M, Jo M, Jung S J and Hwang H 2007 *Appl. Phys. Lett.* **90** 193512
[12] Tseng R J, Tsal C, Ma L, Ouyang J, Ozkan C S and Yang Y 2006 *Nat. Nanotechnol.* **1** 72
[13] Kern W 1993 *Handbook of Semiconductor Wafer Cleaning Technology: Science, Technology, and Applications* (New Jersey: William Andrew)
[14] Malynych S, Luzinov I and Chumanov G 2002 *J. Phys. Chem.* B **106** 1280
[15] Teranishi T, Hosoe M, Tanaka T and Miyake M 1999 *J. Phys. Chem.* B **103** 3818
[16] Daniels J K and Chumanov G 2005 *J. Electroanal. Chem.* **575** 203
[17] Moulder J F, Stickle W F, Sobol P E and Bomben K D 1992 *Handbook of X-ray Photoelectron Spectroscopy* (Minnesota: Physical Electronics)
[18] Chen G L, Li Y, Lin J, Huan C H A and Guo Y P 1999 *Surf. Interface Anal.* **28** 245
[19] Tan Z, Samanta S K, Yoo W J and Lee S 2005 *Appl. Phys. Lett.* **86** 013107
[20] Liou J J-W, Hyang C-J, Chen H-H and Hong G 2003 *IEEE Trans. Electron Devices* **50** 995