Guided self-assembly of Au nanocluster arrays electronically coupled to semiconductor device layers

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We report the controlled deposition of close-packed monolayer arrays of $\sim$5-nm-diam Au clusters within patterned regions on GaAs device layers, thus demonstrating guided self-assembly on a substrate which can provide interesting semiconductor device characteristics. Uniform nanometer scale ordering of the clusters is achieved by a chemical self-assembly process, while micron scale patterning is provided by a soft lithographic technique. Scanning tunneling microscope imaging and current–voltage spectroscopy indicate the Au nanoclusters are strongly coupled electronically into the underlying semiconductor substrate while exhibiting only weak electronic coupling in the lateral plane. © *2000 American Institute of Physics.* [S0003-6951(00)00329-6]

Self-assembly techniques can realize nanoscale ordering and can replace conventional lithographic techniques, which become expensive and slow when used to define nanoscale features. A number of self-assembly techniques have been reported for fabricating nanoscale assemblies of clusters, quantum dots, and wires.[1–6] In order to realize devices and/or circuits with functionalities comparable to conventional integrated circuits, however, it is necessary to break the symmetry of uniform self-assembled networks in controlled ways, e.g., to provide structures which supply gain, nonuniform interconnects, and directionality. Since semiconductor devices can provide the gain essential for regenerative logic functions and directionality, the electronic integration of self-assembled networks of nanoscale elements with semiconductor device structures is of particular interest. An architectural configuration using such an approach has been described using cells consisting of two-dimensional networks of nanoscale metallic nodes on active semiconductor mesas with well-defined local intercell connections.[7] It therefore would be interesting to combine nanoscale self-assembly ordering of metal clusters on a semiconductor substrate with a procedure which can impose a desired larger-scale pattern to form cells and interconnections. Approaches for using molecular tether layers[8] and regions patterned by photoresist[9,10] to deposit individual nanoclusters on solid surfaces have been reported. However, the studies reported to date have not realized well ordered structures such as close-packed monolayer arrays of nanoclusters and strong electronic coupling between the nanoclusters and a semiconductor substrate.

In this paper we describe a guided self-assembly approach, which can realize structures consisting of close-packed monolayer arrays of gold nanoclusters ($\sim$5 nm in diameter) selectively deposited in patterned regions on a GaAs semiconductor surface with strong electronic coupling between the nanoclusters and the semiconductor substrate. In order to achieve well-ordered nanoscale arrays within microscale regions of arbitrary pattern and strong electronic coupling to the substrate, we have employed a resistless lithography procedure involving deposition of an organic tether molecule on a chemically stable semiconductor surface layer. The method involves (i) the deposition of a monolayer of an organic tether molecule in pre-defined regions on the semiconductor substrate, (ii) the transfer of a large-area close-packed array of alkanethiol encapsulated Au nanoclusters onto the substrate, and (iii) a solvent rinse to remove nanoclusters in regions not coated with the tether molecule.

The GaAs device layers used for this study, grown by molecular beam epitaxy on a GaAs(100) substrate, are illustrated in Fig. 1. The top layer is Be-doped low-temperature grown GaAs (LTG:GaAs),[11] which provides a more chemically stable surface (with respect to stoichiometric GaAs), thereby allowing the formation of a relatively stable organic monolayer.[12] A monolayer of xylyl dithiol (HS–CH$_2$–C$_6$H$_4$–CH$_2$–SH, denoted as XYL) is deposited in

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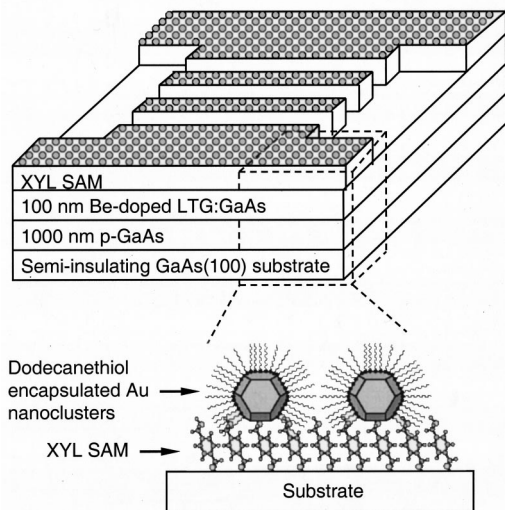[c)]Author to whom all correspondence should be addressed.

FIG. 1. Schematic of close-packed arrays of Au nanoclusters deposited in patterned regions on a LTG:GaAs surface using directed self-assembly fabrication. The monolayer arrays of Au nanoclusters are present only in regions coated with a tether molecule (XYL).
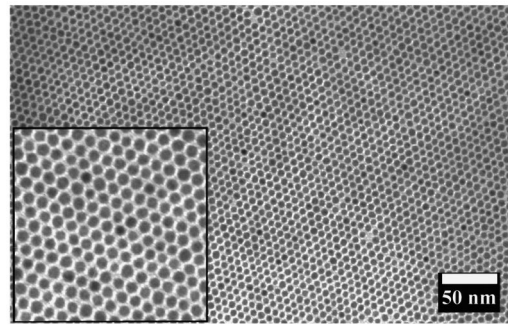

FIG. 2. A TEM micrograph of a hexagonal close-packed monolayer array of Au nanoclusters transferred from a water surface to a carbon TEM grid. The inset is a 100×100 nm enlarged view of this cluster array.

predefined regions on the LTG:GaAs substrate using microcontact printing.[13] This double-ended thiol molecule provides both strong tethering and electronic coupling of nanoclusters to the LTG:GaAs surface.[12] Conventional photoresist based techniques[9,10] are not suitable for the present application due to the associated nonplanarity of the resist covered surface, potential for molecular level contamination, and possibility of reactions between the chemicals used in photoresist processing and the Au nanoclusters.

A well-ordered cluster monolayer is formed by spreading a solution of dodecanethiol encapsulated Au nanoclusters in hexane onto a water surface.[14] The solution contains approximately 2×10^{14} clusters/ml and is spread at room temperature onto a convex water surface formed by containing the water in a cylindrical Teflon™ cell. Sufficient solution is used to just cover the water surface. As the hexane evaporates, a uniform monolayer film of clusters nucleates at the center of the water surface and spreads to the wall of the cell. The central region of this monolayer film is transferred to the XYL patterned substrate by briefly touching the substrate's surface to the film.[15] The local and long-range order of the cluster monolayer is verified by transferring a section of the film to an amorphous carbon membrane supported on a copper grid and imaging the array in a transmission electron microscope (TEM). As shown in Fig. 2, a TEM micrograph of a transferred monolayer reveals a high-quality, hexagonal close-packed array of Au nanoclusters, with a center-to-center distance between neighboring clusters of 8.3 ± 0.8 nm. The translational order of the cluster array is preserved over several microns, with a point vacancy density of $\sim 10^{-4}$ times the cluster density of $\sim 2 \times 10^{12}$ clusters/cm^2.

After transferring the well-ordered cluster film to the patterned LTG:GaAs substrate, the substrate is rinsed in hexane to wash off the clusters not tethered by XYL. A scanning electron microscopy (SEM) image of the resulting sample is shown in Fig. 3(a). The pattern in Fig. 3(a) replicates the pattern of the elastomer stamp pad. The dark areas in the image are covered by clusters and are the areas coated with XYL.

The nanometer scale ordering of the clusters within the regions coated with XYL and the electronic coupling between the clusters and the GaAs surface are investigated using an ultrahigh vacuum (UHV) scanning tunneling microscope (STM). Well-ordered hexagonal close-packed arrays are observed [Fig. 3(b)], with a center-to-center distance between clusters of 7.9 ± 0.6 nm. The well-defined, stable STM images verify that an ordered array is transferred to the LTG:GaAs surface and that the clusters are well tethered mechanically to the surface. Although the limited scan size of the high resolution STM (~ 0.1 μm) and the lack of a means to controllably move the stage in micron scale steps prevent simultaneous observation of the nanometer scale cluster ordering and the lithographically defined micron scale pattern, STM scans at various locations are consistent with the interpretation that a well-ordered, dense array is selectively deposited in the XYL-coated regions. In scans at arbitrary positions on the sample surface, either a close-packed array of clusters or no evidence of any clusters or cluster arrays is observed.

The measured STM current–voltage relationships shown in Fig. 4 indicate that strong electronic coupling can be obtained between the Au clusters and the doped GaAs, provided that an appropriate semiconductor structure is used. The solid curve in Fig. 4 is taken over a cluster in a patterned array sample with the semiconductor structure shown in Fig. 1. Since the Be-doped LTG:GaAs layer is relatively thick (100 nm), the cluster-to-semiconductor resistance is domi-
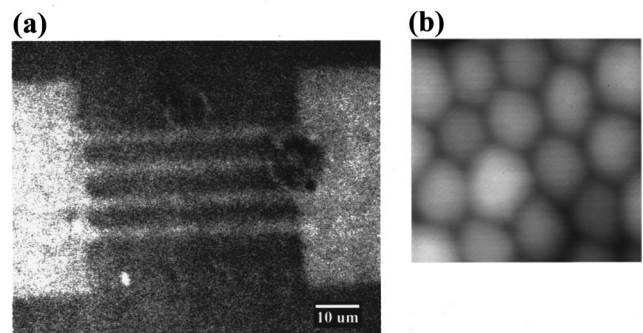
(a)   **(b)**

FIG. 3. (a) A SEM micrograph of a patterned Au nanocluster array on LTG:GaAs. The light colored regions are bare LTG:GaAs and the dark colored areas are regions covered by Au nanoclusters. (b) A 30×30 nm UHV STM topographic image of the Au nanoclusters in the XYL defined regions on the LTG:GaAs substrate ($I_{set} = 200$ pA and $V_{set} = -1.5$ V).
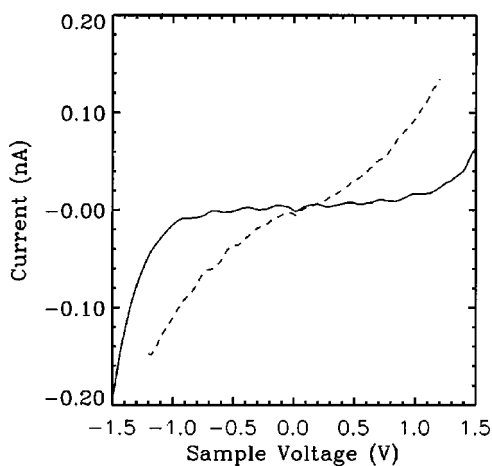
FIG. 4. UHV STM $I-V$ data taken over representative Au clusters in monolayer arrays of nanoclusters tethered to two different XYL-coated GaAs substrates. The solid curve is from a patterned array on a GaAs structure with a 100-nm-thick LTG:GaAs surface layer ($I_{set}=0.2$ nA and $V_{set}=-1.5$ V). The dashed curve is from an unpatterned array on a GaAs structure with a 10-nm-thick LTG:GaAs surface layer ($I_{set}=0.15$ nA and $V_{set}=-1.2$ V).

nated by the bulk resistivity of this layer (approximately 10 Ω cm).[16] A specific contact resistance, $\rho_c \cong 1 \times 10^{-4}$ Ω cm^2, is estimated for this structure, and a substantial fraction of the voltage applied between the tip and the substrate is dropped across the cluster-to-semiconductor interface. Changes in the conductance versus tip bias are expected for this case, since the barrier between the cluster and the semiconductor is changed significantly.

In order to realize a low-resistance cluster-to-semiconductor contact, an unpatterned cluster array was deposited (using the same procedure described previously) onto a XYL-coated GaAs substrate with a 10-nm-thick, Be-doped LTG:GaAs on $n++$GaAs layer, i.e., the structure used in a low-resistance nanocontact.[12] In this case, the combination of the thin LTG:GaAs layer and the $n++$ doped layer results in a thin tunnel barrier between the Au cluster and the doped GaAs layer, and therefore in a low-resistance contact.[17] The specific contact resistance (ρ_c) of this structure is estimated to be $\sim 1 \times 10^{-7}$ Ω cm^2.[12] The measured $I-V$ curve taken over a cluster on this sample (the dashed curve in Fig. 4) shows an enhancement of the low-field conductance and a relatively small conductance change with applied bias, in comparison to the sample with a thick LTG:GaAs layer. Two factors contribute to this behavior. First, a smaller fraction of the applied bias is dropped across the cluster-to-semiconductor interface. Second, a quantitative model for this type of contact structure[17] indicates that the conduction is dominated by tunneling via thermionic-field emission, so the $I-V$ curve is approximately linear for cluster-to-semiconductor biases that are modest compared to the barrier height.

The $I-V$ curves obtained for clusters in the transferred

arrays are comparable to those obtained for isolated clusters.[12] This observation is consistent with the fact that adjacent clusters within the arrays are separated from each other by dodecanethiol, which results in weak intercluster coupling. If adjacent clusters within the array were linked with a conductive molecule,[1] it is expected that the intercluster resistance could be made comparable to the cluster-to-substrate resistance.

In summary, we have deposited patterned networks of Au nanoclusters (~ 5 nm in diameter) on LTG:GaAs semiconductor device layers using a guided self-assembly technique. Well-ordered arrays of the nanoclusters have been observed within regions patterned on the micron scale with a molecular tether (XYL) and strong electronic coupling has been realized between the nanoclusters and the GaAs substrate. The guided self-assembly technique used to fabricate these structures has the potential to provide high-throughput fabrication of structures for future nanoelectronics and other nanoscale applications.

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