IOP Publishing Nanotechnology
Nanotechnology 28 (2017) 135201 (8pp) https://doi.org/10.1088/1361-6528/aa5f0d

Attachable and flexible aluminum oxide resistive non-volatile memory arrays fabricated on tape as the substrate

Woocheol Lee, Jingon Jang, Younggul Song, Kyungjune Cho, Daekyoung Yoo, Youngrok Kim, Seungjun Chung[1] and Takhee Lee[1]

Department of Physics and Astronomy, and Institute of Applied Physics, Seoul National University, Seoul 08826, Republic of Korea

E-mail: seungjun@phya.snu.ac.kr and tlee@snu.ac.kr

Received 23 November 2016, revised 31 January 2017
Accepted for publication 7 February 2017
Published 27 February 2017

Abstract

We fabricated 8 × 8 arrays of non-volatile resistive memory devices on commercially available Scotch® Magic™ tape as a flexible substrate. The memory devices consist of double active layers of Al_2O_3 with a structure of Au/Al_2O_3/Au/Al_2O_3/Al (50 nm/20 nm/20 nm/20 nm/50 nm) on attachable tape substrates. Because the memory devices were fabricated using only dry and low temperature processes, the tape substrate did not suffer from any physical or chemical damage during the fabrication. The fabricated memory devices were turned to the low resistance state at ~3.5 V and turned to the high resistance state at ~10 V with a negative differential resistance region after ~5 V, showing typical unipolar non-volatile resistive memory behavior. The memory devices on the tape substrates exhibited reasonable electrical performances including a high ON/OFF ratio of 10^4, endurance over 200 cycles of reading/writing processes, and retention times of over 10^4 s in both the flat and bent configurations.

Supplementary material for this article is available online

Keywords: attachability, flexibility, resistive memory, non-volatility, negative resistance

(Some figures may appear in colour only in the online journal)

1. Introduction

Recently, resistive random access memory has attracted considerable attention as a promising memory device [1–3] due to its advantages including a fast process, low power consumption, and high density integration ability. In particular, it allows the use of simple architectures with electro-controllable bistable resistance layers between top and bottom electrodes. A variety of materials such as oxide-based materials [4–6], nitride-based materials [7–9], and organic materials [10–12] have been used as the resistive switching layer. Among these candidates, aluminum oxide (Al_2O_3) was employed as an active layer material because it could be deposited by using an e-beam evaporation system at relatively low temperature [13]. Al_2O_3 has gained interest as an active layer due to its good reliability and controllability [14, 15]. Although there are many previously reported results of resistive memory devices using Al_2O_3 layers, further improved electrical performances are highly desirable, particularly for endurance or electrical stability. In this regard, using doped oxide layers [16, 17], inserting metal layers into the active layer [15], or using different oxide layers that are sequentially deposited [18, 19] have been conducted to deliver better electrical characteristics. In these efforts, inserting a metal layer in the active layer can be regarded as an effective and facile approach to improving the electrical stability of the resistive memory devices.

In addition, because the demands for new electronic applications, such as wearable electronics, have increased, there have been considerable efforts to demonstrate flexible device applications [20–22]. In this manner, a use of organic materials has attracted much attention to realize soft

[1] Authors to whom any correspondence should be addressed.

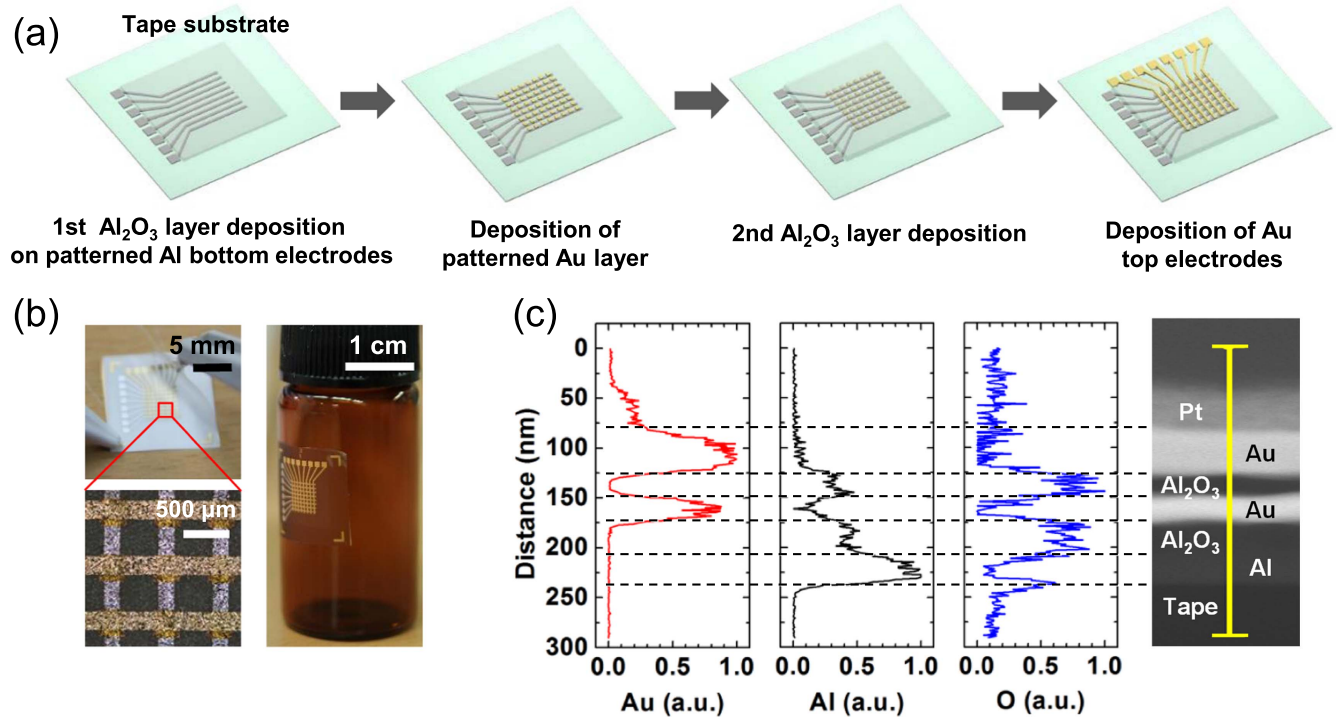

Figure 1. (a) Fabrication procedure of the memory devices on Scotch® Magic™ tape as a substrate. (b) Photographic and optical microscope images of the memory devices. (c) A cross-sectional TEM image with specified element percentage graphs along the yellow line.

electronics due to their great flexibility, low-cost, and low-temperature processability. However further enhancements respecting to operation voltages and environmental reliability are still required for practical applications. Recently, inorganic layers, especially metal oxide layers with tens of nm thickness have been widely employed as a switching layer to realize flexible memory devices [23]. This strategy can address aforementioned issues of organic materials even though metal oxide materials have relatively less mechanical flexibility.

Additionally, low-cost processes are highly desirable for the realization of future disposable electronics such as electronic tags, labels, and newspapers [24, 25]. However, silicon-based electronic devices cannot be fabricated on low-cost flexible platforms due to their high-temperature processes and chemical additive processes. Moreover, to develop disposable memory device applications, the use of cost-effective materials and fabrication methods is required on low-cost platforms, such as paper or polymer substrates. In this regard, research groups have demonstrated disposable field effect transistors on various paper substrates [26–28]. Our group also reported metal oxide-based resistive memory devices on wrapping paper [29]; however, there have been no attempts to realize individually operated memory arrays on these advanced platforms.

Here, we report aluminum oxide resistive non-volatile memory devices realized on commercially available Scotch® Magic™ tape substrates, which provides good attachability to a wide range of materials. The resistive memory devices in cross-bar arrays were fabricated using low-temperature processes to minimize physical or thermal damage to the tape substrates. To improve the electrical stability, a metallic layer was inserted in the Al_2O_3 active layers. The fabricated memory arrays exhibited unipolar resistive switching behavior with high ON/OFF ratios, good endurance, and good retention in both the flat and bending configurations.

2. Experimental details

A conventional tape (Scotch® Magic™ tape, 3M Inc.) was used as the substrate. Before fabrication, we confirmed from a thermal test that the tape could not endure temperatures over 120 °C (see figure S1 which is available at stacks.iop.org/NANO/28/135201/mmedia in the supplementary data). Therefore, low-temperature processes were used for the device fabrication. For convenient fabrication, the tape was attached to a smooth paper surface from which the tape could easily be detached. The tape substrates were cleaned by rubbing with isopropyl alcohol soaked cotton swabs. After the rubbing, the substrates were dried by blowing N_2 for ~30 s. Figure 1(a) shows a schematic of the device fabrication process. The eight lines of the Al bottom electrodes were deposited through a shadow mask on the tape substrate by thermal evaporation with a deposition rate of 0.5 Å s^{-1} and at a pressure of $\sim 10^{-6}$ Torr. The thickness and width of the Al bottom electrode line was 50 nm and 200 μm, respectively.

One Al_2O_3 layer can act as a resistive memory layer [30–32]; however, the endurance and yield of the memory devices could be improved by inserting a metal layer between

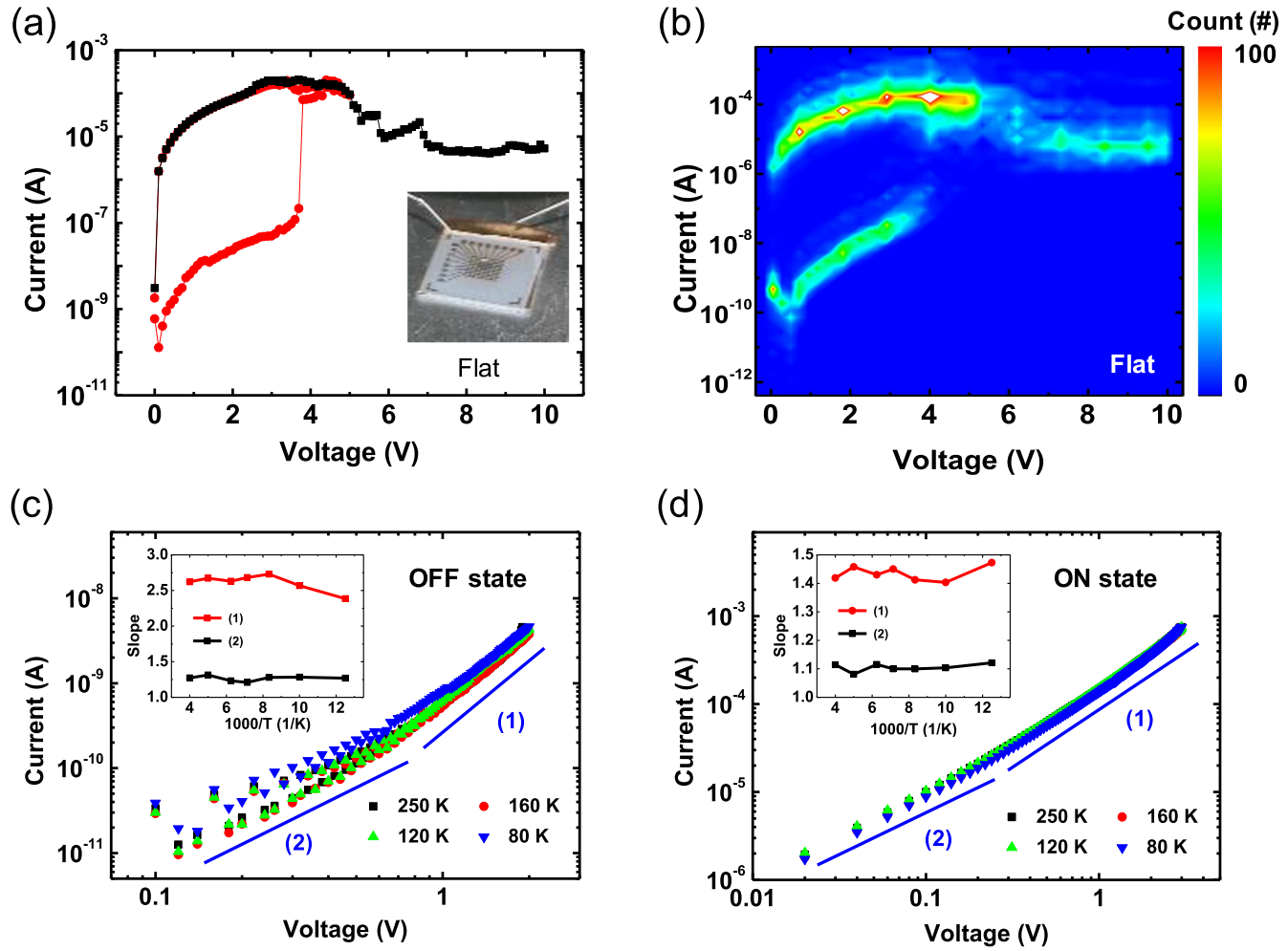

Figure 2. (a) Representative current–voltage graph of a memory device in the flat condition. (b) Color map of the current–voltage graphs of 65 memory devices. A double-log plot analysis of the current–voltage characteristics at various temperatures in (c) ON state and (d) OFF state. Inset graphs are slops versus $1000/T$ (T: temperature).

the Al_2O_3 layers [15]. Al_2O_3 is usually deposited by atomic layer deposition (ALD). However, the ALD process requires a temperature of 200 °C; the tape substrate will be surely damaged at this temperature. Thus, we used an e-beam evaporator, which can deposit materials at room temperature. The layers of Al_2O_3, Au, Al_2O_3, and Au (20 nm/20 nm/20 nm/50 nm) were deposited sequentially by the electron-beam evaporator at the same pressure and with the same deposition rate as the deposition conditions of the Al bottom electrodes. The first Al_2O_3 layer was deposited covering all eight lines of the Al bottom electrodes. Then, the Au layer was deposited through a shadow mask forming 64 square cells (see figures 1(a) and (b)). Next, the second Al_2O_3 layer, which has the same thickness as the first Al_2O_3 layer, was deposited. Last, the Au top electrode was deposited by the electron-beam evaporator using the same conditions. The top electrodes had the same patterns as the bottom electrodes but crossed the bottom electrode lines orthogonally in the cross-bar array architecture. After the deposition processes, the tape substrates were cut into 1.5 × 1.5 cm^2 pieces using scissors. Because tape was used as the substrate, the fabricated devices can easily stick to any surface. The right image of figure 1(b) shows that the fabricated memory devices stick vertically on the curved wall of a vial.

Figure 1(c) shows the cross section transmission electron microscope (TEM) image of a memory device with the proportion of each element along the cross section. We could verify that Au was deposited as the top electrode and the active layer between the Al_2O_3 layers from the Au proportion graph. The O-rich parts indicate the Al_2O_3 active layers, which were well-deposited without aggregation or defects even though they were formed by the low-temperature thermally vaporized process using an e-beam evaporator. The bottom Al_2O_3 layer was thicker than the top Al_2O_3 layer, because the Al bottom electrode was naturally oxidized forming an Al_2O_3 film. The Pt on the Au top electrode layer was deposited as a protection layer for the focused ion beam process, which was needed to make the specimen for TEM examination.

The electrical properties of the memory devices were measured with a semiconductor parameter analyzer (Model

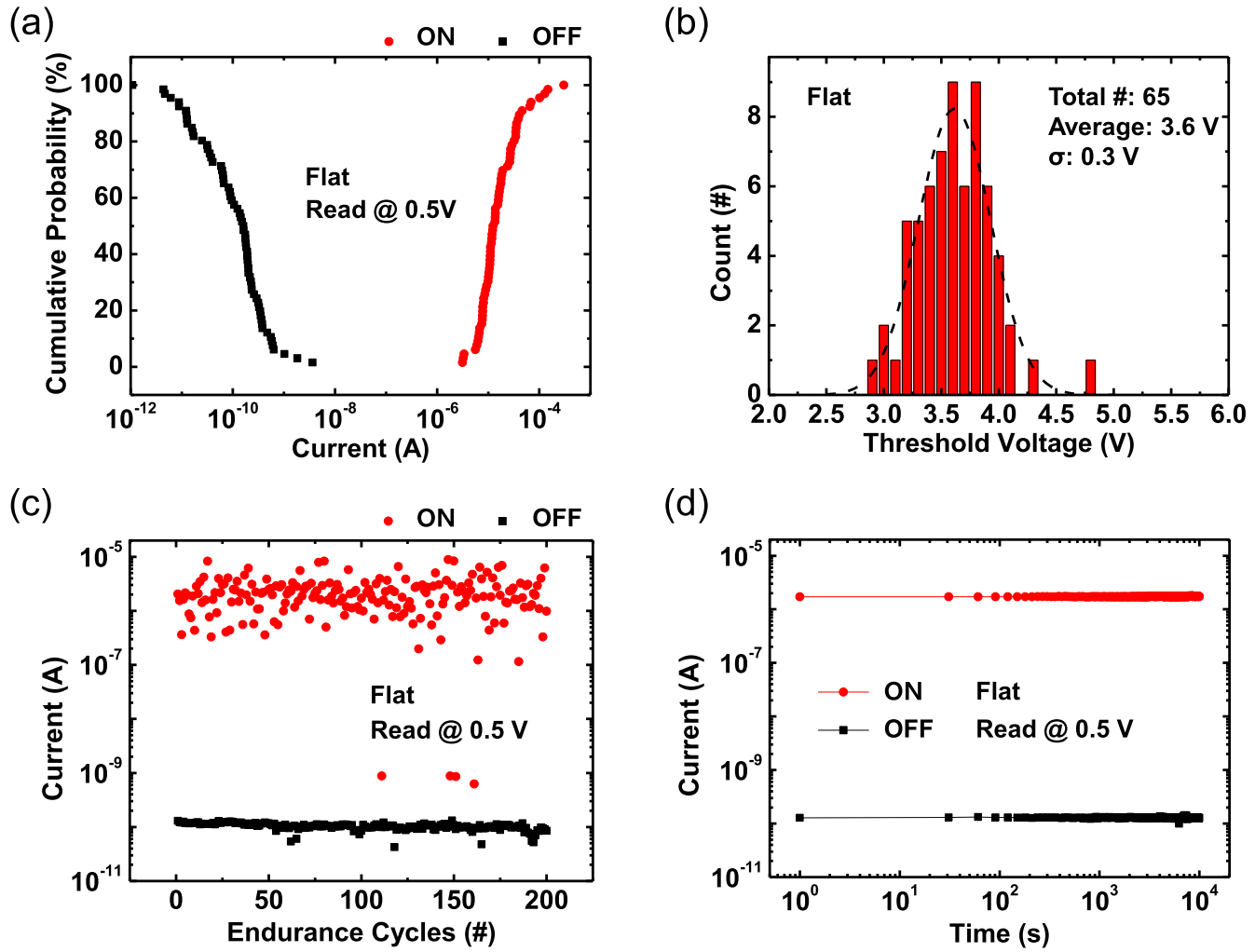

Figure 3. (a) The cumulative probability of the memory devices in the flat condition at a read voltage of 0.5 V. (b) The distribution of the threshold voltages. (c) Endurance test and (d) retention test results of the memory devices.

4200 SCS, Keithley Inc.) inside a N_2 filled glove box at room temperature. To measure the electrical characteristics in the flat and bent conditions, the memory devices were attached on glass substrates and semi-cylinders, respectively.

3. Results and discussion

Figure 2(a) shows the representative electrical properties of the memory devices. The inset is a photograph of the memory devices on the tape being measured in the flat condition. To make the ON state (low resistance state), forward and backward sweeping voltages were applied from 0 to 5 V and then from 5 to 0 V. The current jumped swiftly from the OFF state (high resistance state) to the ON state around ~4 V. The ON state was maintained as long as a low voltage was applied, which means the memory devices have a non-volatile memory characteristic. To make the devices in the OFF state, we swept the voltage from 0 to 10 V. The current was reduced after ~5 V, showing a negative differential resistance region [33, 34]. After this, the current was maintained in the OFF state at low voltage. As a result, the device had two controllable stable states so that it can be used as a rewritable non-volatile memory. The ON/OFF ratio was found to be high enough (~10^4) at a read voltage of 0.5 V. We examined a total of 94 memory device cells and confirmed 65 cells worked well (device yield of ~70%). Figure 2(b) shows a color map of the current–voltage graphs of all 65 working memory cells, which confirms that the memory window between the ON and OFF states was large enough statistically. Additionally, figure 2(b) shows that the OFF currents of most devices abruptly changed to ON currents. Note that the failure of ~30% devices showed either short currents or only OFF state currents.

Many research groups have explained charge transport mechanism in resistive switching memory devices with space charge limited current (SCLC), Poole–Frenkel conduction, and Fowler–Nordheim tunneling [35–37]. We previously explained that Poole–Frenkel conduction and SCLC were dominant for the charge transport in a similar metal oxide memory system [29]. For the clear understanding, we performed variable temperature measurements, as the results are

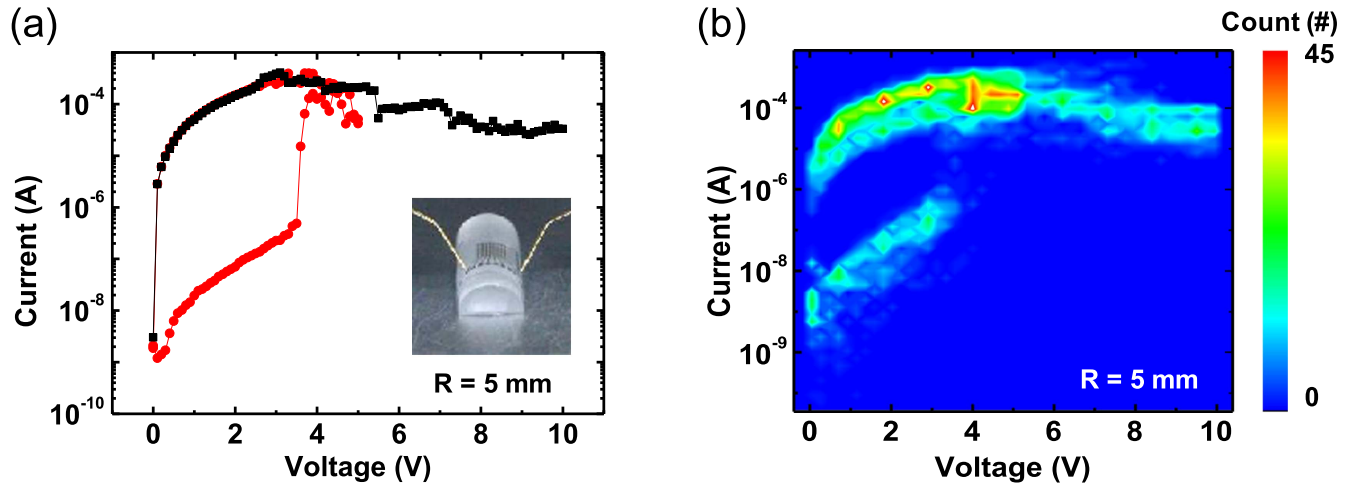

Figure 4. (a) Representative current–voltage graph of a memory device in the bent condition with a bending radius of 5 mm. (b) Color map of current–voltage graphs of 30 memory devices.

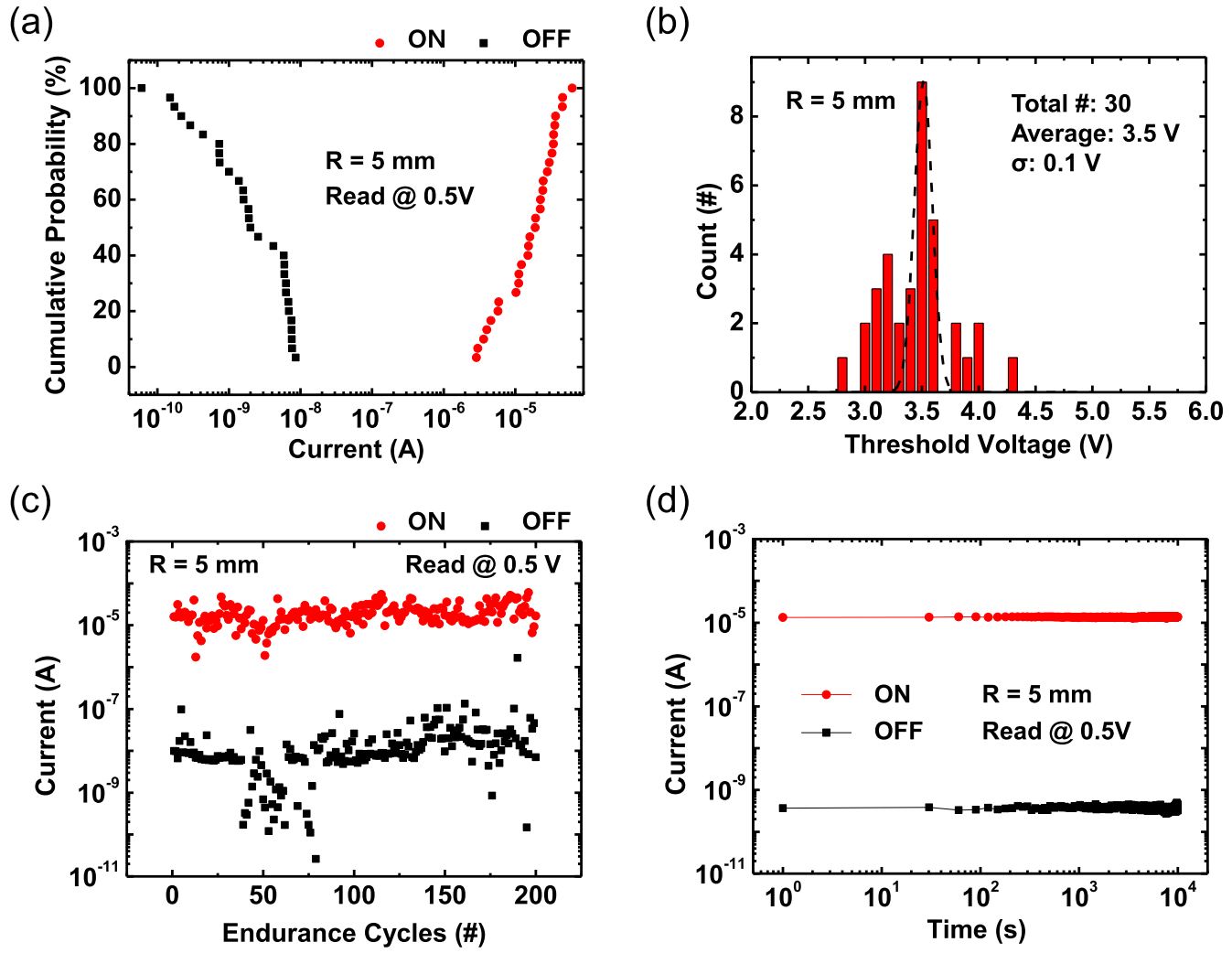

Figure 5. (a) The cumulative probability of the memory devices in the bent condition with a bending radius of 5 mm at read voltages of 0.5 V. (b) The distribution of threshold voltages. (c) Endurance test and (d) retention test results of the memory devices.

shown in figures 2(c) and (d). The bias was swept from 0 to 2.5 V for the OFF state and from 0 to 3 V for the ON state. As it can be seen from these figures, we did not observe noticeable temperature dependence of the current–voltage (I–V) characteristics in both ON and the OFF states. Because SCLC and Poole–Frenkel conduction are dependent on

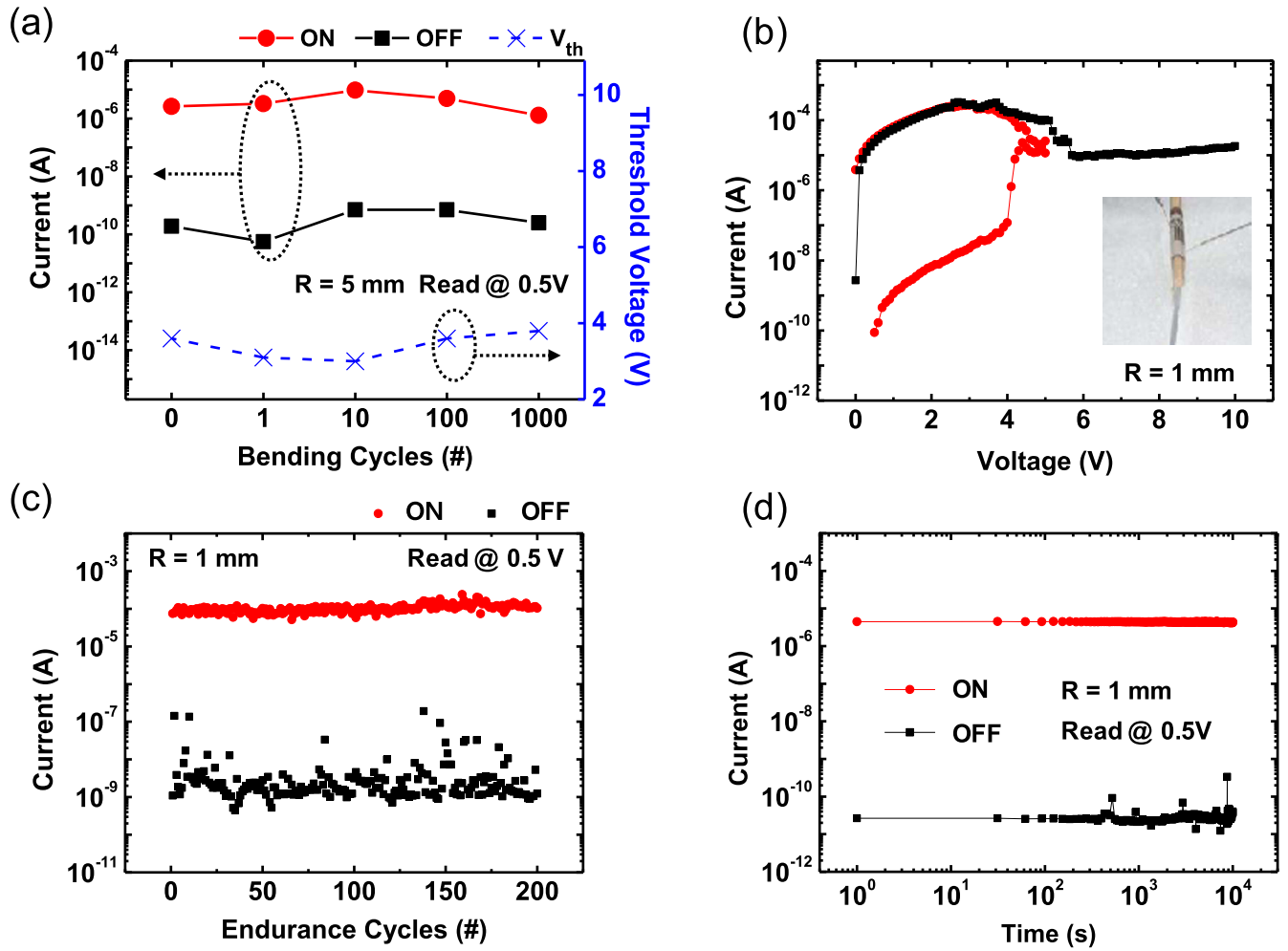

Figure 6. (a) Bending cycle test with a bending radius of 5 mm. (b) Representative current–voltage graph of a memory device with a bending radius of 1 mm. (c) Endurance test and (d) retention test results of the memory devices with a bending radius of 1 mm.

temperature, the charge transport mechanism in our memory device might not be explained solely by SCLC or Poole–Frenkel conduction. The temperature-independent transport properties may suggest tunneling conductions through trap sites in the switching layer [38]. Therefore, we propose a traps-associated tunneling (see figure S2 in the online supplementary data). However, clearer understanding of the switching and conduction mechanisms will require further investigations.

One of the important characteristics of memory devices is reliability. We tested the reliability using statistical methods. Figure 3(a) shows the ON and OFF currents of 65 memory device cells at 0.5 V. We could find that the lowest ON current was over two orders of magnitude higher than that of the highest OFF current. This indicates that the memory devices had two stable states at the read voltage. Figure 3(b) shows the distribution of the threshold voltage values, which are the voltages required to turn the devices to the ON state. The average threshold voltage was found to be ∼3.6 V with a standard deviation of ∼0.3 V. This small distribution of threshold voltages indicates that the memory devices had statistical uniformity. Figure 3(c) shows the endurance test results of the memory devices. The ON states were achieved by applying 5 V, which is sufficiently higher than the threshold voltage of ∼3.6 V. Then, the OFF states were achieved by applying 10 V for approximately 0.1 s. The read voltage was 0.5 V. The memory devices maintained the wide memory window of three to four orders of magnitude between ON and OFF states for over 200 cycles of ON and OFF states. Although there were several failures to turn on (see some scattered red data points in figure 3(c)), it did not mean the memory device had broken. Figure 3(d) shows the retention test results of a memory device. The read voltage was 0.5 V and the reading interval was 30 s for both the ON and OFF states. The currents of both the ON and OFF states were stably maintained for $\sim 10^4$ s with a high ON/OFF ratio of $\sim 10^4$. Note that the performances of these memory devices on the tape substrate were comparable to those of the memory devices fabricated on another plastic substrate, OHP film (see figure S3 in the online supplementary data).

To investigate the electrical properties of the memory devices in bending conditions, we attached the devices on a semi-cylinder with a radius of 5 mm and performed the same measurements that were conducted on the memory devices in

the flat conditions. Figure 4(a) is the representative electrical characteristics of a memory device in the bent condition. Similar *I–V* characteristics were observed in the flat and bent conditions (see figures 2 and 4). We investigated a total of 47 memory device cells in the bent condition. The device yield was found to be ∼64% (30 of 47), which was slightly lower than that (∼70%) in the flat condition. The color map in figure 4(b) shows that the large memory window was well maintained in the bent condition.

The cumulative probability graph (figure 5(a)) shows that the high ON/OFF ratio at read voltage was maintained in the bent condition. The distribution of the threshold voltages was also similar to that for the flat condition (figure 5(b)). The average and the standard deviation of the threshold voltage were found to be ∼3.5 V and ∼0.1 V, respectively. The memory devices on the curved surface still endured 200 cycles of ON/OFF. Although the ON/OFF ratio was slightly degraded and the deviation of the OFF currents became larger than in the memory devices on the flat surface (figure 5(c)), the devices maintained two well-separated stable states. Figure 5(d) also supports that the bending did not have any noticeable harmful influence on the retention characteristics of the memory devices. Also, during 1000 cycles of bending-relaxation at a bending radius of 5 mm, the devices maintained a high ON/OFF current ratio of $\sim 10^4$ with threshold voltage of ∼3.5 V and no significant changes of the switching behaviors were observed during this measurement (see figure 6(a)). And, the memory devices well maintained their electrical properties including the ON/OFF state currents and threshold voltages under a harsh bending condition with a bending radius of 1 mm, as shown in figure 6(b). Moreover, the memory devices exhibited good retention time of $\sim 10^4$ s and stable switching-operation during the 200 cycles of bending-relaxation at the bending radius of 1 mm (see figures 6(c) and (d)). All these results suggest that our memory devices on the tape substrate can be attached on any curved surface within the bending radius of 1 mm without serious performance degradation.

4. Conclusion

In summary, we fabricated resistive memory device arrays on conventional Scotch® Magic™ tape substrates using dry and low temperature processes. The attachable memory devices showed typical unipolar resistive switching properties with good electrical performance in both flat and bent configurations. The memory devices endured 200 cycles of switching and maintained their states for over 10^4 s with a high ON/OFF ratio ($\sim 10^4$). The attachable memory device arrays fabricated on flexible and disposable tape substrates may provide a pathway for the realization of practical and reliable resistive memory applications such as disposable electronic tags, labels, and sticker memory devices.

Acknowledgments

This work was accomplished through the financial support from the National Creative Research Laboratory Program (grant No. 2012026372) provided by the National Research Foundation of Korea (NRF) grant which is funded by the Korean Ministry of Science, ICT & Future Planning.

References

[1] Waser R and Aono M 2007 *Nat. Mater.* **6** 833
[2] Kwon D-H *et al* 2010 *Nat. Nanotechnol.* **5** 148
[3] Lee M-J *et al* 2011 *Nat. Mater.* **10** 625
[4] Akinaga H and Shima H 2010 *Proc. IEEE* **98** 2237
[5] Sawa A 2008 *Mater. Today* **11** 28
[6] Wong H-S P, Lee H-Y, Yu S, Chen Y-S, Wu Y, Chen P-S, Lee B, Chen F T and Tsai M-J 2012 *Proc. IEEE* **100** 1951
[7] Kim H-D, An H-M, Kim K C, Seo Y, Nam K-H, Chung H-B, Lee E B and Kim T G 2010 *Semicond. Sci. Technol.* **25** 065002
[8] Chen C, Gao S, Tang G, Song C, Zeng F and Pan F 2012 *IEEE Electron Device Lett.* **33** 1711
[9] Kim H-D, An H-M, Lee E B and Kim T G 2011 *IEEE Trans. Electron Devices* **58** 3566
[10] Cho B, Song S, Ji Y, Kim T W and Lee T 2011 *Adv. Funct. Mater.* **21** 2806
[11] Wang C, Gu P, Hu B and Zhang Q 2015 *J. Mater. Chem.* C **3** 10055
[12] Lee T and Chen Y 2012 *MRS Bull.* **37** 144
[13] Madaan N, Kanyal S S, Jensen D S, Vail M A, Dadson A E, Engelhard M H, Samha H and Linford M R 2013 *Surf. Sci. Spectra* **20** 43
[14] Pan F, Gao S, Chen C, Song C and Zeng F 2014 *Mater. Sci. Eng.* R **83** 1
[15] Song J *et al* 2010 *Appl. Phys. Express* **3** 091101
[16] Kim W, Park S I, Zhang Z, Yang-Liauw Y, Sekar D, Wong H-S P and Wong S S 2011 *VLSI Symp. on Tech. Dig.* p 22 http://ieeexplore.ieee.org/abstract/document/5984614/
[17] Wu Y-T, Jou S and Yang P-J 2013 *Thin Solid Films* **544** 24
[18] Kim K M, Choi B J, Koo B W, Choi S, Jeong D S and Hwang C S 2006 *Electrochem. Solid-State Lett.* **9** G343
[19] Wang L-G, Qian X, Cao Y-Q, Cao Z-Y, Fang G-Y, Li A-D and Wu D 2015 *Nanoscale Res. Lett.* **10** 1
[20] Cai Y, Tan J, YeFan L, Lin M and Huang R 2016 *Nanotechnology* **27** 275206
[21] Cramer T, Travaglini L, Lai S, Patruno L, de Miranda S, Bonfiglio A, Cosseddu P and Fraboni B 2016 *Sci. Rep.* **6** 38203
[22] Jang B C, Seong H, Kim S K, Kim J Y, Koo B J, Choi J, Yang S Y, Im S G and Choi S-Y 2016 *ACS Appl. Mater. Interfaces* **8** 12951
[23] Sun Y and Rogers J A 2007 *Adv. Mater.* **19** 1897
[24] Forrest S R 2004 *Nature* **428** 911
[25] Tobjörk D and Österbacka R 2011 *Adv. Mater.* **23** 1935
[26] Kim Y-H, Moon D-G and Han J-I 2004 *IEEE Electron Device Lett.* **25** 702
[27] Zocco A T, You H, Hagen J A and Steckl A J 2014 *Nanotechnology* **25** 094005
[28] Zschieschang U, Yamamoto T, Takimiya K, Kuwabara H, Ikeda M, Sekitani T, Someya T and Klauk H 2011 *Adv. Mater.* **23** 654
[29] Jang J, Song Y, Cho K, Kim Y, Lee W, Yoo D, Chung S and Lee T 2016 *Flex. Print. Electron.* **1** 034001

[30] Lin C-Y, Wu C-Y, Wu C-Y, Hu C and Tseng T-Y 2007 *J. Electrochem. Soc.* **154** G189
[31] Hubbard W, Kerelsky A, Jasmin G, White E R, Lodico J, Mecklenburg M and Regan B C 2015 *Nano Lett.* **15** 3983
[32] Zhu W, Chen T P, Liu Z, Yang M, Liu Y and Fung S 2009 *J. Appl. Phys.* **106** 093706
[33] Simmons J G and Verderber R R 1967 *Proc. R. Soc.* A **301** 77
[34] Kim T W, Zeigler D F, Acton O, Yip H L, Ma H and Jen A K Y 2012 *Adv. Mater.* **24** 828
[35] Spahr H, Montzka S, Reinker J, Hirschberg F, Kowalsky W and Johannes H-H 2013 *J. Appl. Phys.* **114** 183714
[36] Chang W-Y, Lai Y-C, Wu T-B, Wang S-F, Chen F and Tsai M-J 2008 *Appl. Phys. Lett.* **92** 022110
[37] Lee H Y *et al* 2009 *IEEE Electron Device Lett.* **30** 703
[38] Yu S, Guan X and Wong H-S P 2011 *Appl. Phys. Lett.* **99** 063507