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Electrical Properties of Synthesized Large-Area MoS_2 Field-Effect Transistors Fabricated with Inkjet-Printed Contacts

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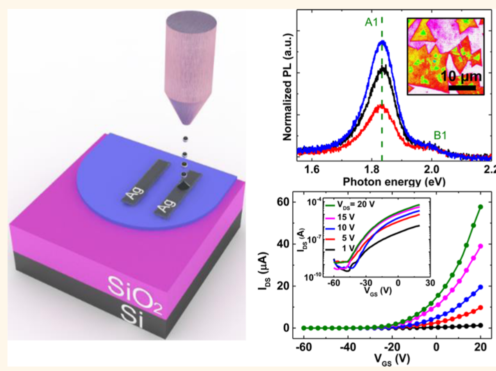
Supporting Information

ABSTRACT: **We report the electrical properties of synthesized large-area monolayer molybdenum disulfide (MoS_2) field-effect transistors (FETs) with low-cost inkjet-printed Ag electrodes. The monolayer MoS_2 film was grown by a chemical vapor deposition (CVD) method, and the top-contact Ag source/drain electrodes (S/D) were deposited onto the films using a low-cost drop-on-demand inkjet-printing process without any masks and surface treatments. The electrical characteristics of FETs were comparable to those fabricated by conventional deposition methods such as photo- or electron beam lithography. The contact properties between the S/D and the semiconductor layer were also evaluated using the Y-function method and an analysis of the output characteristic at the low drain voltage regimes. Furthermore, the electrical instability under positive gate-bias stress was studied to investigate the charge-trapping mechanism of the FETs. CVD-grown large-area monolayer MoS_2 FETs with inkjet-printed contacts may represent an attractive approach for realizing large-area and low-cost thin-film electronics.**



KEYWORDS: *molybdenum disulfide, field-effect transistors, inkjet printing, contact resistance, gate-bias stress effect, electronic transport properties*

Two-dimensional (2D) transition metal dichalcogenides (TMDCs) have attracted much attention due to their great potential monolayer applications in opto- and nanoelectronics.[1−4] Among various TMDC materials, molybdenum disulfide (MoS_2) has been most widely studied because the atomically thin (~0.65 nm) monolayer MoS_2 exhibits an excellent transparency in the visible wavelength range, mechanical stiffness, flexibility, and electrical carrier mobility.[5−7] In particular, contrary to zero-band-gap graphene, MoS_2 shows a transition from indirect band gap (~1.2 eV) to direct band gap (~1.8 eV), with decreasing thickness from bulk to monolayer, which allows higher efficiency in photogeneration and recombination. Therefore, large-area monolayer MoS_2 is a promising material to use in optoelectronic devices, such as photodetectors, light-emitting diodes (LEDs), and solar cells.[8−10]

Various methods for the preparation of a monolayer MoS_2, such as mechanical exfoliation, chemical exfoliation, physical vapor deposition (PVD), and chemical vapor depositions (CVD), have been recently reported.[11−13] To meet the growing demand for large-area electronics, synthetic fabrication methods to produce a large-area monolayer MoS_2 are highly desirable because a large-area monolayer MoS_2 cannot be consistently obtained using conventional mechanical or chemical exfoliation methods. Among these synthetic fabrication methods, the CVD method with molybdenum trioxide (MoO_3) and sulfur powder has enabled high-quality MoS_2 film deposition on largely selected regions and controllable thickness with excellent electrical characteristics.[14−17]

To design source/drain (S/D) electrodes, electron beam (e-beam) or photolithography techniques have been widely used on the nanometer-thick MoS_2. Unfortunately, these processes, which require unwanted procedures such as chemicals deposition, ultraviolet (UV) exposure, and contact contaminations, can degrade the electrical properties of devices and are also not suitable for large-area flexible platforms. In this regard, an inkjet-printing process, which has been proposed for large-

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area, low-cost, and ambient electronics, such as organic thin-film transistors (TFTs), organic light-emitting diodes (OLEDs), oxide TFTs, and sensors, is believed to be a promising candidate for top-contact electrode formation due to its low-cost, nonvacuum character, and large-area process abilities.[18−21] For the printed electrode formation on monolayer MoS_2, low-cost Ag ink can be a good candidate in terms of electron injection because the work function of Ag (∼4.26) is equivalent to that of Ti (∼4.33), which is widely used as a contact metal with n-type semiconductor layers. To date, however, there has been no report regarding monolayer MoS_2 field-effect transistors (FETs) with inkjet-printed Ag S/D due to the difficulties in optimizing the inkjet-printing process and compatibility between printable inks and the bottom monolayer MoS_2.

Herein, we report the first demonstration of large-area monolayer MoS_2 FETs with inkjet-printed Ag S/D electrodes. The monolayer MoS_2 film was grown by a CVD system, and the Ag electrodes were inkjet-printed using a commercial drop-on-demand (DOD) printer, which allows for the realization of large-area and low-cost electronics. The metallic ink for the S/D formation was carefully selected by considering the wetting and contact properties of the underlying MoS_2 film. The predominantly monolayer character of the CVD-grown MoS_2 film was verified by atomic force microscopy (AFM), Raman, and photoluminescence (PL) spectroscopy measurements. The electrical properties of the MoS_2 FETs with the printed S/D, including field-effect mobility and on/off ratio, were comparable to those of the FETs with conventionally deposited contacts using e-beam or photolithography processes. The wetting and contact properties between the Ag contacts and the MoS_2 semiconductor layer were also investigated by extracting the surface energy and the contact resistance. Moreover, the electrical instability of the MoS_2 FET was investigated under a prolonged positive gate-bias stress to verify the charge-trapping mechanism between the CVD-grown monolayer MoS_2 and the SiO_2 gate dielectric. This study for the integration with large-area CVD-grown monolayer MoS_2 films and low-cost inkjet-printed contacts can have a strong impact in the fields of 2D TMDC nano- and optoelectronics.

RESULTS AND DISCUSSION

Figure 1a presents a representative optical image of a synthesized monolayer MoS_2 on a heavily doped Si/SiO_2 substrate by a CVD system (Teraleader Co., Ltd.). In this optical image, the synthesized MoS_2 and the no-growth regions are colored dark violet and light violet, respectively. It is well-known that a large number of individual MoS_2 triangular islands that are few tenths of a micrometer in size are merged into a continuous film[22] (MoS_2 triangular islands and continuous film are shown in the right and left part of Figure 1a, respectively). The thickness of the individual MoS_2 triangular islands was measured using a non-contact-mode AFM (Park systems, NX 10), as shown in Figure 1b. The cross-sectional topographic profile indicated by the cyan line included in Figure 1b indicates a thickness of ∼0.7 nm along the blue straight line; this measurement is consistent with the previously reported thickness of CVD-grown MoS_2. Raman and PL spectra measurements were performed on the CVD-grown MoS_2 film to clarify the spatial uniformity and the number of layers. Details of the experiments are presented in the Methods section and Figure S1 of Supporting Information.

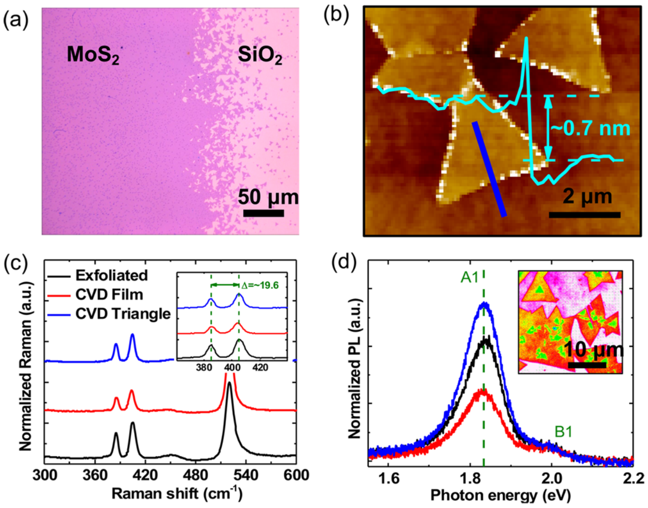

Figure 1. (a) Optical micrograph of CVD-grown monolayer MoS_2 (left area) and a no-growth SiO_2 (right area) substrate. (b) AFM image of CVD-grown monolayer MoS_2 triangular islands (the profile indicates the thickness of triangular islands along the blue line). (c) Raman spectra of three different MoS_2 samples. (d) PL spectra of three different points of CVD-grown films. The inset image shows a linear scale PL image of triangular islands.

Figure 1c shows Raman spectra from three different MoS_2 samples: CVD-grown MoS_2 film (red curve), MoS_2 triangular island (blue curve), and mechanically exfoliated monolayer MoS_2 flakes (black curve). The CVD-grown MoS_2 triangular island and film showed Raman spectra similar to that of a mechanically exfoliated monolayer MoS_2 flake (SPI Supplies, USA) on the SiO_2 (270 nm) substrate measured as a reference, including a strong Si peak at approximately 528 cm^{-1}. The expected monolayer MoS_2 Raman peak spacing of ∼19.6 cm^{-1} from the out-of-plane A_{1g} (385.2 cm^{-1}) and in-plane E^1_{2g} (404.8 cm^{-1}) peaks was clearly observed on all three MoS_2 samples, as shown in the inset of Figure 1c.[23,24] For further investigation, PL spectra, intensity, and peak position mappings were measured for three different points on the CVD-grown large-area MoS_2 film. Figure 1d shows the identical strong A1 peaks around a photon energy of ∼1.83 eV that originated from direct band-to-band recombination of excited electron−hole pairs and relatively weak B1 at approximately 2.0 eV. This result is also consistent with the previous publication which supports a MoS_2 single-layer PL property.[25−27] The linear scale PL image of the CVD-grown MoS_2 triangular islands in thhe inset of Figure 1d substantiates the excellent optical properties of monolayer MoS_2. The PL peak position mapping of the CVD-grown MoS_2 film also showed good uniformity across a few hundred micrometers (see Figure S1 of Supporting Information).[28,29] These results strongly support that the CVD-grown MoS_2 film was predominantly composed of monolayers.

Figure 2a shows the procedure of fabricating inkjet-printed silver (Ag) electrodes onto the large-area CVD-grown monolayer MoS_2, along with a representative optical image (the MoS_2 film and Ag electrodes are colored dark violet and white in the optical image, respectively). For the formation of the top S/D electrodes, a nanoparticle-type Ag ink (DGP 40LT-15C, ANP Co. Ltd.) containing 32 wt % Ag was printed onto the synthesized MoS_2 films using a DOD piezoelectric inkjet printer (DMP-2831, Dimatix Corp.), and then, the electrodes were sintered at 180 °C for 30 min on a hot plate under ambient condition. Because the Ag ink showed good

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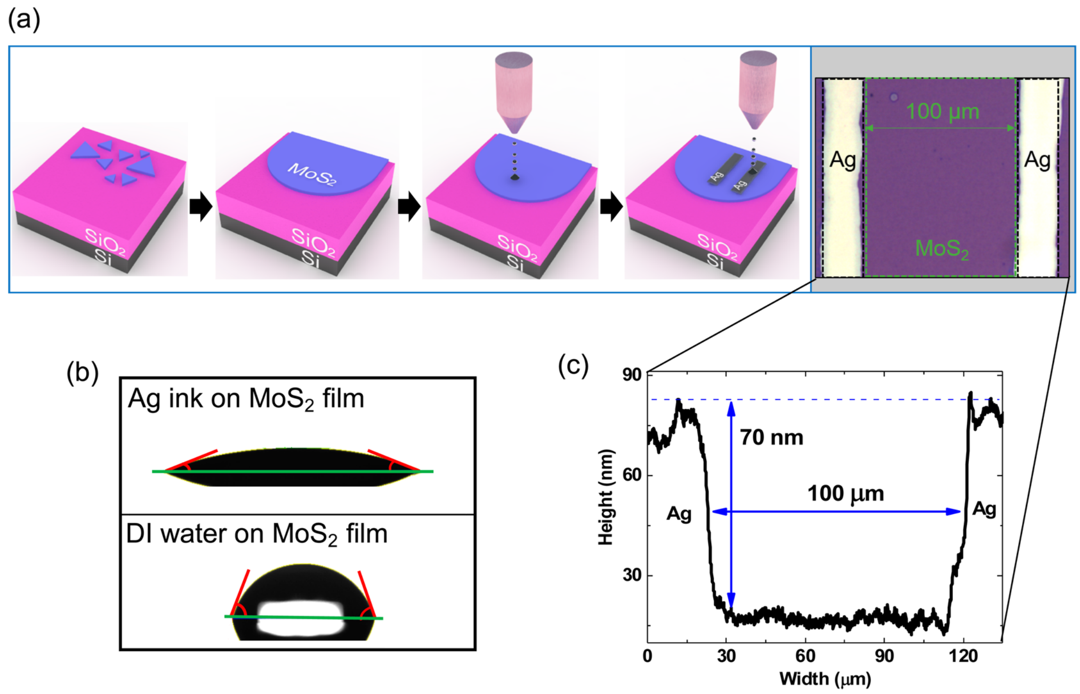

Figure 2. (a) Schematic illustrations and a representative optical image (in gray background) of the fabrication of CVD-grown monolayer MoS_2 FETs with inkjet-printed Ag electrodes. (b) Representative optical images of sessile drops on CVD-grown monolayer MoS_2 film. The top and bottom images show the Ag ink and DI water drops on the MoS_2 film, respectively. (c) Surface profiles of CVD-grown monolayer MoS_2 films with inkjet-printed Ag electrodes.

wetting property on the CVD-grown MoS_2 film without any surface treatments, as shown in Figure 2b, nozzles with a small diameter of 9 μm that eject a 1 pL volume of ink drops were used; therefore, the S/D were well-defined without the coffee-ring effect, bulging, or edge waviness. The surface energy of the CVD-grown MoS_2, which determines the wetting property, was also studied to verify the compatibility with the Ag ink. Notably, the Ag ink drops were similarly dispersed on the CVD-grown MoS_2 film and the no-growth SiO_2 regions, which indicates that both the CVD-grown monolayer MoS_2 and the no-growth SiO_2 surfaces have similar surface energies. Hence, the contact angles for polar deionized (DI) water, dispersive diiodomethane (CH_2I_2), and the Ag ink were measured under ambient conditions to determine the surface energy of the CVD-grown monolayer MoS_2 film and the no-growth SiO_2 substrates (see Table 1). If a sessile drop is on the surface, then

Table 1. Contact Angles (deg) of Different Liquids on CVD-Grown Monolayer MoS_2 and No-Growth SiO_2 Surfaces

liquids	DI water	CH_2I_2	Ag ink
no-growth (SiO_2)	58.5	42.6	19.8
CVD-grown monolayer MoS_2	75.2	24.5	14.4

the balance on the three phases (liquid, solid, and gas) can be expressed in Young's equation:

$$\gamma_S = \gamma_{SL} + \gamma_L \cos\theta \qquad (1)$$

where γ_S, γ_L, γ_{SL}, and θ denote the solid surface tension, liquid surface tension, interfacial tension between the solid and liquid, and contact angle between the surface and liquid−gas interface, respectively. Among various surface energy calculation methods originated from Young's equation, a two-component Owens−Wendt method (Owens−Wendt geometric mean equation) was used in this study:

$$(1 + \cos\theta)\gamma_L = 2\left(\sqrt{\gamma_S^D \gamma_L^D} + \sqrt{\gamma_S^P \gamma_L^P}\right) \qquad (2)$$

where superscript D and P denote the dispersion and polar components, respectively.[30,31] Figure 2b shows the captured images of the Ag ink and the DI water sessile drops on the CVD-grown MoS_2 film. The measured contact angles between the solid−liquid line (green line) and the gas−liquid line (red line) were ~14 and ~75°, respectively. From eq 2 and the contact angle values in Table 1, the calculated surface energies of the CVD-grown MoS_2 film and the no-growth SiO_2 were 44.07 and 48.06 mN/m, respectively, and these values are comparable to the previously reported value of 48.3 mJ/m^2 (=mN/m) for monolayer MoS_2 from different surface energy calculation methods.[32] The surface profiles of the MoS_2 film channel and printed electrodes were measured using a surface profilometer (Dektak 6M, Veeco). The well-defined printed S/D electrodes had a width and height of 25 μm and 70 nm, respectively (Figure 2c), and exhibited high conductivity (1.2 Ω/sq). The channel length and width were 100 and 300 μm, respectively. The single droplet made a circle having a diameter of 25 μm when it dropped on the CVD-grown MoS_2 films, and we can assume that the highest resolution (or the width of printed electrodes) is 25 μm if the drop-spacing (*i.e.*, a space between adjacent droplets) is carefully optimized.

The electrical properties were characterized using a semiconductor parameter analyzer (4155C, Agilent Technologies) under ambient condition. In particular, all measurements were performed in a dark box to avoid the contribution of the photocurrent in the CVD-grown MoS_2 FETs.[33,34] Figure 3a shows the transfer characteristics (drain−source current *versus* gate−source voltage, I_{DS}−V_{GS}) measured for drain−source

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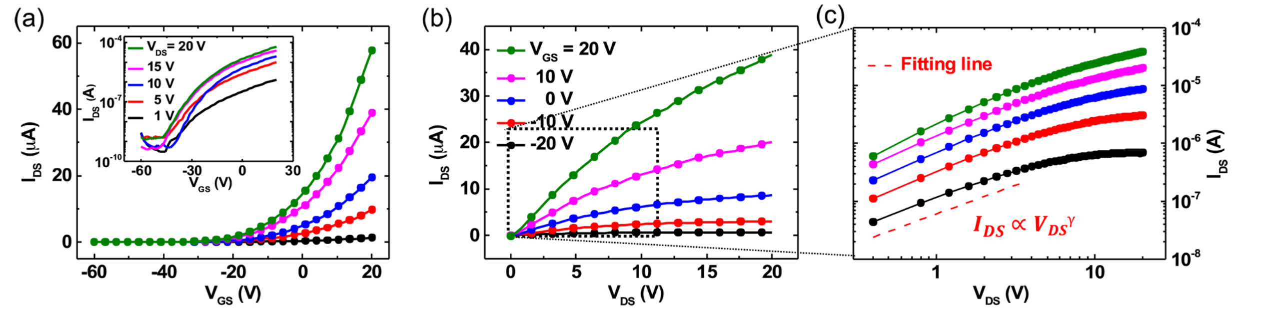

Figure 3. Representative electrical characteristics of the CVD-grown monolayer MoS_2 FET with the inkjet-printed Ag electrodes. (a) Transfer characteristics (I_{DS}−V_{GS}) measured at different V_{DS}. The inset shows the same transfer characteristics on a log scale. (b) Output characteristics (I_{DS}−V_{DS}) measured at different V_{GS}. (c) Log−log plot of output characteristics in the low V_{DS} region. The red dashed lines indicate the fitting line to the $I_{DS} \propto V_{DS}^{\gamma}$ relationship.

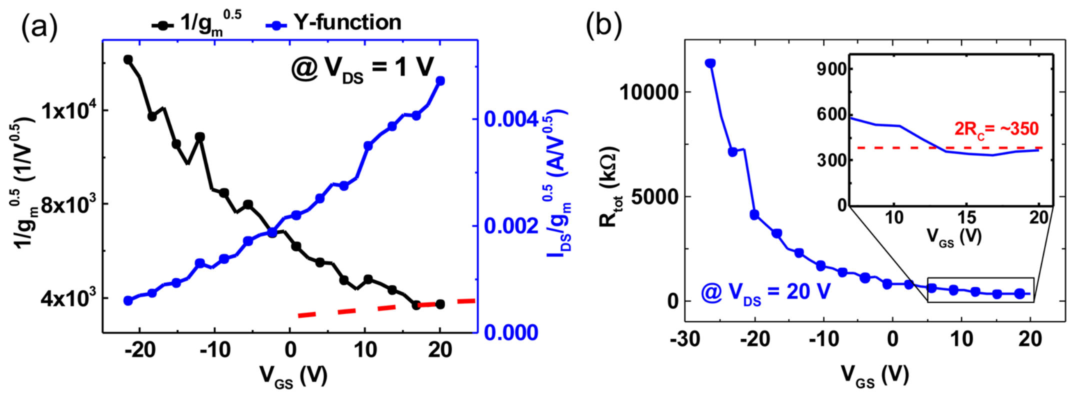

Figure 4. (a) $1/\sqrt{g_m}$ and Y-function ($I_{DS}/\sqrt{g_m}$) of the CVD-grown monolayer MoS_2 FET with inkjet-printed electrodes at V_{DS} of 1 V. (b) Graph of the total resistance (R_{tot}) *versus* the V_{GS} graph at V_{DS} of 20 V; the enlarged image shows the R_{tot} at V_{GS} from 5 to 20 V. The red dashed line shows the slope around V_{GS} of 15 V.

voltage (V_{DS}) ranging from 1 to 20 V by sweeping V_{GS} from −60 to +20 V. The results showed the typical n-type semiconductor behavior with a field-effect mobility (μ_{FE}) of 1.8 $cm^2/V{\cdot}s$ and on/off ratio of greater than 10^4 at V_{DS} of 1 V. The inset in Figure 3a shows the logarithmic scale plot of the transfer characteristics. Considering the reported μ_{FE} values of 1 to 45 $cm^2/V{\cdot}s$ for CVD-grown monolayer MoS_2 FETs at room temperature,[35] several factors are believed to deteriorate the μ_{FE} of the devices in this study. The electrical characteristic measurements performed in ambient condition would cause lower charge transport due to oxygen or water absorption on the semiconductor surface that can deplete electrons, resulting in the degradation of the channel conductivity.[36,37] In addition, intrinsic structural defects in CVD-grown MoS_2 films, such as grain boundaries and point defects, and the interfacial states between the MoS_2 layer and SiO_2 surface could limit the charge transport, as well.[35,38,39] The electrical properties can, therefore, be improved by optimizing the structural quality of the CVD-grown monolayer MoS_2, employing passivation layers onto the channel, and transferring the CVD-grown MoS_2 films onto dangling-bond-free hexagonal boron nitride substrates to minimize the interfacial traps.[40−42] However, the key advantage of a use of inkjet-printed Ag contacts on a large-area CVD-grown MoS_2 film lies not on the electrical performance improvement but on the low-cost drop-on-demand deposition.

Figure 3b shows the output characteristics (drain−source current *versus* drain−source voltage, I_{DS}−V_{DS}) measured at V_{GS} ranging from −20 to +20 V in increments of 10 V by sweeping V_{DS} from 0 to 20 V. The output characteristics revealed good linearity at the low V_{DS} regime. In the relationship $I_{DS} \propto V_{DS}^{\gamma}$ in the logarithmic scale plot, as shown in Figure 3c, the average γ (linearity parameter) value of ~1.1 was found to be close to 1, indicating the formation of an ohmic contact between the CVD-grown MoS_2 film and the printed Ag electrodes. For further investigation, the contact resistance values between the channel and the printed S/D were also extracted because the contact properties strongly affect the electrical characteristics.[7,43]

Although transmission line measurement, also called transfer length method, is widely used to evaluate contact resistance of FETs, it cannot be conveniently employed because several transistors with various channel lengths and uniform contacts are necessary to extract the accurate value. Due to these limitations, the Y-function method (YFM) was proposed for the contact resistance extraction between the CVD-grown monolayer MoS_2 FET and the Ag-printed contacts, as shown in Figure 4a. YFM has been widely used to analyze the contact resistance and intrinsic mobility (μ_0) in the low V_{DS} linear regime ($V_{GS} - V_{th} \gg V_{DS}$) for both organic and carbon-nanotube-based FETs.[44−47] Recently, Chang *et al.* reported that YFM can also be a robust method to extrapolate the contact resistances of nanometer-thick MoS_2 FETs.[48] Generally, I_{DS} in a linear region can be described by

$$I_{DS} = \frac{W}{L} C_i \mu_{eff} (V_{GS} - V_{th}) V_{DS} = \frac{W}{L} C_i \frac{\mu_0}{1 + \theta(V_{GS} - V_{th})} (V_{GS} - V_{th}) V_{DS} \tag{3}$$

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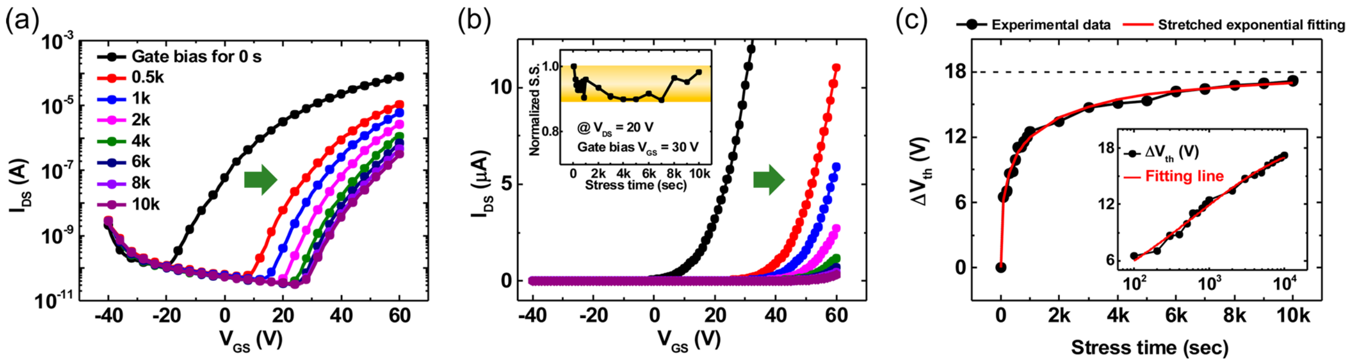

Figure 5. Transfer characteristics measured in ambient conditions with respect to the different gate-bias stress time up to 10 000 s on (a) log and (b) linear scales. The gate-bias stress voltage V_{GS} was 30 V. The inset of (b) shows the change of normalized subthreshold swing (S.S.) with respect to the stress time. (c) Threshold voltage shift (ΔV_{th}) with respect to the value of prestress curve. The solid red line represents a stretched exponential fitting to the experimental data using eq 6. The inset figure shows the ΔV_{th} on a log scale.

where μ_{eff}, μ_0, C_i, V_{th}, W, L, and θ denote the effective mobility in linear regime, the intrinsic mobility, the capacitance between the channel and the gate per unit area, the threshold voltage, the channel width, the channel length, and the mobility attenuation coefficient, respectively. According to the definition of transconductance ($g_m = \partial I_{DS}/\partial V_{GS}$), the Y-function can be defined as

$$\begin{aligned} Y &\equiv \frac{I_{DS}}{\sqrt{g_m}} \\ &= \sqrt{I_{DS}}\sqrt{(V_{GS} - V_{th})\{1 + \theta(V_{GS} - V_{th})\}} \\ &= \sqrt{\mu_0 C_i V_{DS}\frac{W}{L}}(V_{GS} - V_{th}) \end{aligned} \tag{4}$$

From the slope of the Y-function, the extrapolated μ_0 value at V_{DS} = 1 V, which is independent of the attenuating factors, was 2.1 cm^2/V·s, which is 17% larger than the measured μ_{FET} of 1.8 cm^2/V·s. The mobility attenuation factor θ can be described by the following equation:

$$\theta = \theta_{ch} + \theta_c = \theta_{ch} + \mu_0 C_i R_C \frac{W}{L} \tag{5}$$

where θ_{ch}, θ_c, and R_C denote the mobility attenuation factor from the channel, such as a surface roughness and phonon scattering; mobility attenuation factor from the contact; and the contact resistance, respectively. Assuming that θ_{ch} is negligible,[44,48,50] the value of θ is ∼0.02 and the contact resistance of 115 kΩ can be extracted at high V_{GS} from the slope of the Y-function (the red dashed line in Figure 4a). The contact resistance value is relatively higher than the reported contact resistance values of the MoS_2 devices fabricated with various methods (Figure S3b of the Supporting Information). However, these contact resistance values cannot be compared fairly due to several reasons (see the detailed discussion in the Supporting Information).

The extracted contact resistance is also consistent with the saturated total resistance of 175 kΩ at sufficiently large V_{DS} and V_{GS}, where the contribution of the contact resistance is much more dominant than that of the channel (Figure 4b). This contact resistance value is higher than the reported values[49−51] because unwanted residues from the organic solvent or ligands may limit charge injection from the contacts to the MoS_2 layer during the metallic ink-sintering process. In addition, the quite porous surface of the printed S/D due to the size of Ag nanoparticles (∼35 nm) results in smaller effective contact areas. In particular, increasing evidence has suggested that metal/MoS_2 junction formations depend on not only metal work function but also the chemical reactions at the metal/MoS_2.[7,43] Thus, the contact property of inkjet-printed Ag electrodes on CVD-grown MoS_2 would be different from that of evaporated ones, thus affecting the electrical characteristics of the devices.

The electrical instability was also investigated by measuring the electrical characteristics of the FETs under positive gate-bias stress of 30 V. The transfer characteristics were measured every 500 s for 10 000 s at V_{DS} of 20 V by sweeping V_{GS} from −40 to +60 V while interrupting the gate-bias stress. Figure 5a,b shows the transfer curves on the logarithmic and linear scales, respectively. The curves shifted in the positive gate-bias direction as a function of applied gate-bias stress time. The subthreshold swing and slope of the curves were almost identical to during the measurement (the inset of Figure 5b). These results support that the defect creation of extra electron-trapping states is negligible, whereas the trapped electrons at the MoS_2/SiO_2 interface or bulk dielectric that can reduce the effective gate bias are dominant for the V_{th} instability during positive gate-bias stress. The stress time dependence of the V_{th} shift during a prolonged gate bias was fitted to the stretched exponential equation described as

$$\Delta V_{th} = \Delta V_0\left[1 - \exp\left(-\left(\frac{t_{st}}{\tau}\right)^{\beta}\right)\right] \tag{6}$$

where ΔV_0, τ, β, and t_{st} denote the change of V_{th} after infinite time, the characteristic trapping time, the stretched exponent, and the gate-bias stress time, respectively (Figure 5c). The stretched exponential equation has been developed to quantitatively model the charge-trapping mechanism by injection of carriers from the channel to the near-interface or the bulk dielectric in amorphous silicon (*a*-Si) TFTs.[52] The extrapolated values of ΔV_0, τ, and β were found to be ∼18.1 V, 8.1×10^2 s, and ∼0.413, respectively. The statistical coefficient R^2 value of 0.9937 indicates that experimental data (black closed circles) were well-fitted to the stretched exponential equation fitting line (as the statistical coefficient R^2 is closed to 1, the experimental data are well-fitted to the equation). Notably, the larger τ value compared to that of the mechanically exfoliated MoS_2 FETs[53] indicates the higher trap density in the CVD-grown MoS_2 film or at the interface

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with the dielectric and also can be evidence of a large number of band tail states of the CVD-grown monolayer MoS_2 films.[54]

CONCLUSION

In summary, we report for the first time, to our knowledge, large-area CVD-grown MoS_2 FETs fabricated with low-cost inkjet-printed Ag S/D electrodes and their electrical properties. The CVD-grown monolayer MoS_2 films showed well-defined and uniform Raman and PL spectra, and the inkjet-printed S/D electrodes were deposited successfully onto the MoS_2 films without any surface treatments by optimizing the printing process. The large-area FETs showed electrical characteristics comparable to those of MoS_2 FETs with conventionally deposited contacts at room temperature under ambient conditions. The contact property between the MoS_2 and printed Ag electrodes was also analyzed using the Y-function method. Furthermore, the charge-trapping mechanism was primarily responsible for the electrical instability, especially the V_{th} shift, of CVD-grown monolayer MoS_2 FETs under positive gate-bias stress. This study provides a promising pathway for integrating CVD-grown large-area monolayer MoS_2 FETs with a low-cost inkjet-printing technique.

METHODS

Fabrication of CVD-Grown MoS_2 FETs with Inkjet-Printed Ag Contacts. Monolayer MoS_2 films were grown using a CVD system. We used dual-heating zone system: one for the MoO_3 powders and the Si/SiO_2 substrates (~750 °C) and the other for the sulfur (S) powders (~200 °C). A 270 nm SiO_2 was thermally grown onto each highly p-doped Si substrate. Ar gas was used as a carrier gas. For S/D electrode formation, a nanoparticle-type Ag ink containing 32 wt % Ag (DGP 40LT-15C, ANP Co. Ltd.) and a cartridge that ejects 1 pL of ink droplets were used. After the Ag ink was inkjet-printed at a drop velocity of 8 m/s and a drop-spacing of 30 μm onto a 60 °C substrate using a DMP-2831 (Fuji Films Corp.) printer, the sample was sintered on a 180 °C hot plate for 30 min under atmospheric environment. Note that no more oxidation-related degradations during other fabrication processes or measurements were not observed because the surface of printed Ag conductive layers is slightly oxidized during the sintering process.[55] See the details in Figure S1 of the Supporting Information.

Raman and PL Spectra Measurements. High-resolution PL mapping was performed to characterize the uniformity of CVD-grown films and triangular islands. These measurements were performed with a WITec Alpha 300RA system using the 532 nm line of a frequency-doubled Nd:YAG laser as the excitation source. The spectra were measured in the backscattering configuration using a 100× objective and a 600 grooves/mm grating. Raman spectra were obtained with a 1800 grooves/nm grating. The laser power was 25 μW with a diffraction-limited spot size.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.5b07942.

Synthesis and characterization of CVD-grown monolayer MoS_2, contact angles of DI water and Ag ink drops on SiO_2/Si, Y-function method analysis of CVD-grown monolayer MoS_2 FET, electrical characteristics under illumination, and electrical characteristics of other device on the same back-gate SiO_2 substrate (PDF)

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Notes

The authors declare no competing financial interest.

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