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Performance enhancement of triisopropylsilylethynyl pentacene organic field effect transistors with inkjet-printed silver source/drain electrodes achieved via dispersible reduced graphene oxide

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ABSTRACT

We report a performance enhancement of triisopropylsilylethynyl (TIPS) pentacene organic field effect transistors (OFETs) obtained by treating the surface of SiO_2/Si substrate with dispersible reduced graphene oxide (rGO). The source and drain electrodes were patterned with inkjet-printed highly conductive silver. The sheet resistance of inkjet-patterned silver electrodes has found to be ~1 Ω/□, which is comparable to that of typical vacuum-evaporated silver electrodes. The electrical performance has improved by rGO treatment, with a morphology improved for the active TIPS pentacene layer. The rGO treatment increased the morphological grain size of TIPS pentacene, resulting in a decreased number of interfacial trapping sites in the carrier transport paths. The field effect mobility of the TIPS pentacene OFETs, following the rGO surface treatment, was improved from 0.082 $cm^2/V{\cdot}s$ to 0.141 $cm^2/V{\cdot}s$.

1. Introduction

Organic field effect transistors (OFETs) have been widely studied in recent years due to their simple device architecture, low-cost manufacturing processes, ease of fabrication, flexibility, unlimited variety of available materials, low operating temperatures, and multitude of potential applications [1–3]. A considerable number of focused studies have achieved device performance for OFETs comparable to that of amorphous silicon devices. The device performance and stability of OFETs mainly depend on the electrode/channel and dielectric/channel interfaces [4,5]. To improve carrier transport at the electrode/channel contact, a suitable candidate electrode material has been widely sought to replace the traditionally used expensive Au or indium tin oxide. For example, we previously demonstrated that the device performance of pentacene OFETs using a multilayer graphene film as a source/drain electrode was enhanced over that of an Au-electrode pentacene OFET [6]. Similarly, intensive research has been conducted on improving the dielectric/channel interface to increase device performance. The morphology of the active channel layer in OFETs is closely related to the properties of the gate dielectric/channel interface, acting as a major factor in determining carrier transport in OFETs [5]. For OFETs that use SiO_2 as a back gate dielectric layer, an octadecyltrichlorosilane (OTS) self-assembled monolayer (SAM) treatment has commonly been used to create a more suitable active channel layer morphology to improve OFET mobility [4,7]. OTS surface treatment of the SiO_2 dielectric/channel interface can enhance the device performance of OFETs by improving molecular ordering, grain size, and packing [5,8–10].

Recently, graphene has increased in significance and has been widely studied due to its many advantageous properties such as large-area synthesis, high intrinsic mobility, good thermal and electrical conductivity, and transparency [11,12]. Possessing excellent conduction properties, graphene sheets have commonly been used in electrodes for electronic and photonic devices, including thin film transistors, memory devices, photovoltaic cells, and light-emitting diodes [11,13,14]. Graphene sheets were initially obtained by mechanically exfoliating bulk highly ordered pyrolytic graphite. Currently, epitaxial chemical vapor deposition is generally used to synthesize graphene sheets. However, these routes are less effective for large-scale fabrication, motivating research on graphene materials that can be chemically processed, such as graphene oxide (GO). The use of strong oxidizing agents to produce GO is the most common alternative to graphite exfoliation [15].

In general, GO is synthesized by the Brodie, Staudenmaier, or Hummers method: the GO aromatic lattice contains epoxides, carbonyls, alcohols, and carboxylic groups [16–18]. Unlike graphene, GO has the considerable advantage of being able to be processed in solution and manufactured in bulk, increasing the scope of applications for GO. For example, GO has been used as an active layer in non-volatile resistive memory devices, as a channel layer in thin film FETs, and as a gate dielectric layer in carbon nanotube transistors [15,19–22]. GO can also be used to produce dispersible reduced

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graphene oxide (rGO) through the removal of epoxides and carbonyl groups by a strong reducing agent, such as hydrazine or hydrogen iodide (HI) [23,24]. Although the loss of carbon atoms during reduction results in an incomplete lattice structure, rGO exhibits graphene-like electronic behavior with high chemical and mechanical stability. So it has been widely used as not only the electronic components such as active layer and conducting electrodes but also interfacial electronic contacts preventing the formation of metallic short circuits [23–27].

In this study, we fabricated triisopropylsilylethynyl (TIPS) pentacene OFETs by using dispersible rGO as surface treatment material on SiO_2/Si substrate prior to TIPS pentacene deposition where inkjet-printed silver electrodes were used as the source and drain electrodes. We observed performance enhancement of the OFETs with an rGO coating on SiO_2/Si substrate due to morphological improvements at the dielectric/channel interfaces. The rGO treatment increased the morphological grain size of the TIPS pentacene, reducing the number of interfacial traps in the carrier transport paths. Characterization of the TIPS pentacene OFETs using the well-known OTS SAM treatment showed similar morphological changes in the TIPS pentacene active layer and a similar enhancement in the electrical performance.

2. Experimental details

2.1. Synthesis of reduced graphene oxide

GO powder was prepared from natural graphite powder (Bay Carbon, SP-1 graphite) using the modified Hummers and Offenman method with H_2SO_4, $NaNO_3$, and $KMnO_4$ [18,28]. Four grams of prepared GO was dispersed in 1.5 L of acetic acid. The dispersion was sonicated until it became clear. HI (80 ml) was then added to the mixture, which was stored at 40 °C for 40 h under constant stirring. The product was isolated by filtration and washed with saturated sodium bicarbonate (500 ml), distilled water (500 ml), and acetone (200 ml) before being vacuum-dried overnight at room temperature to yield the rGO powder (~3 g) [29].

2.2. Device fabrication

Fig. 1 shows a schematic of our TIPS pentacene OFET device. To fabricate the devices, first, a Si wafer with a 100-nm-thick SiO_2 layer was cleaned by a standard solvent-cleaning process (using acetone followed by 2-propyl-alcohol (IPA) and then de-ionized (DI) water in an ultrasonic bath for 20 min) and dried at 150 °C for 30 min on a hot plate to evaporate the residual solvent and moisture. The source and drain electrodes were patterned with inkjet-printed highly conductive silver. The advantages of the inkjet printing-based electrode process over the typical vacuum-evaporation electrode process include decreased material wastage, low cost, and scalability to large-area manufacturing [30]. The inkjet patterning process involves printing by a metal-organic solvent precursor-type ink (INKTEC TEC-IJ-010, 15 wt% silver content and 9 ~ 15 cps viscosity) on a piezoelectric inkjet printer (Dimatix DMP 2800). We used only one jetting nozzle, out of 16 nozzles in a silver ink-filled cartridge, to prevent undesirable angular errors in the patterning. The silver ink was printed twice at a drop velocity of approximately 7 m/s, a jetting voltage of approximately 20 V, a drop spacing of 25 μm, a meniscus set point of 2 inches H_2O, a cartridge print height of 1 mm, and a jetting frequency of 5.0 kHz, while the plate temperature and cartridge temperature were maintained at 40 °C and 35 °C, respectively. Following printing of the source/drain electrodes, the substrate was sintered at 150 °C for 30 min on a hot plate. At the moment when the metal-organic silver ink reached on target surface, the shape of ink droplet was maintained instantaneously (the upper image of Fig. 2(a)) because it takes very short time for ink drop to reach on substrate. When the sintering heat was applied, the rigid silver-solvent mass congregated each other with gradual evaporation of solvent, so the amorphous-type silver electrode was formed after sintering (the lower image of Fig. 2(a)). For metal-organic-type silver inks, the printed electrodes are known to begin to appear shiny at temperatures over 120 °C [31].

Fig. 2(b) shows the sheet resistance of the printed silver electrodes as a function of the sintering time. The sheet resistance of conventional thermally evaporated silver electrodes is also shown for comparison. The sheet resistance of the source/drain electrodes of our OFET devices was found to be approximately 1 Ω/□ after 30 min of curing; thus, the conductivity of the printed silver was comparable to that of a vacuum-evaporated silver electrode (~0.7 Ω/□). The thickness of the printed silver was ~300 nm, and the channel width (W) and length (L) of the patterned OFETs were 300 and 100 μm, respectively. After the silver electrodes were inkjet-patterned, a prepared rGO solution (0.1 wt% in *N*-methyl-2-pyrrolidone) was spin-coated at 1000 rpm for 30 sec, before being heated on a hot plate at 60 °C for 30 min to evaporate any residual solvent. Finally, 1 wt% of TIPS pentacene dissolved in anisole was drop-casted, heated at 50 °C for 20 min to form an active

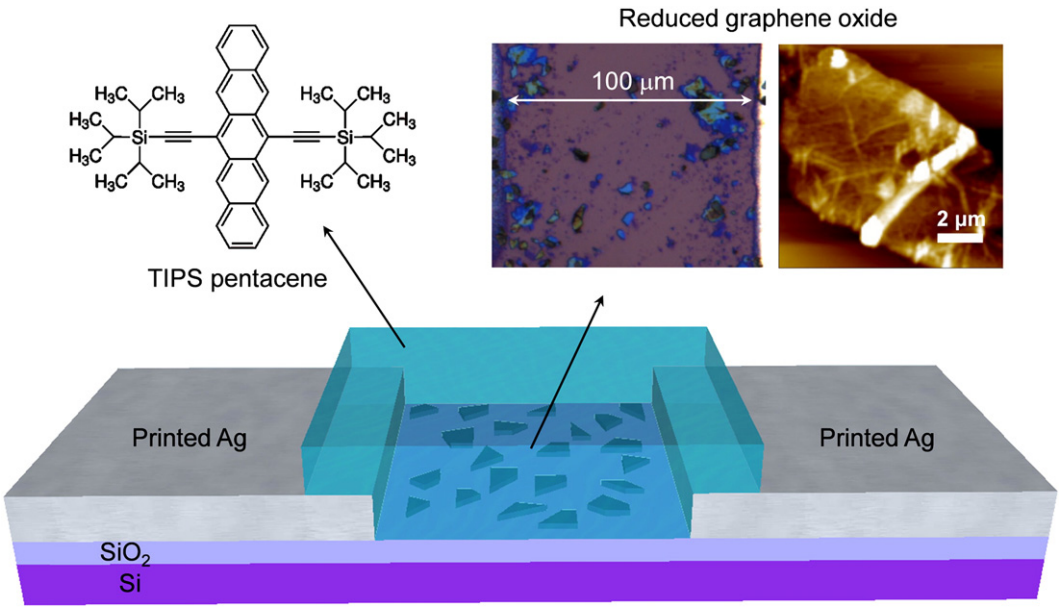

Fig. 1. The schematic of fabricated device. The molecular structure of TIPS pentacene and the optical and AFM image of the dispersible rGO are shown.

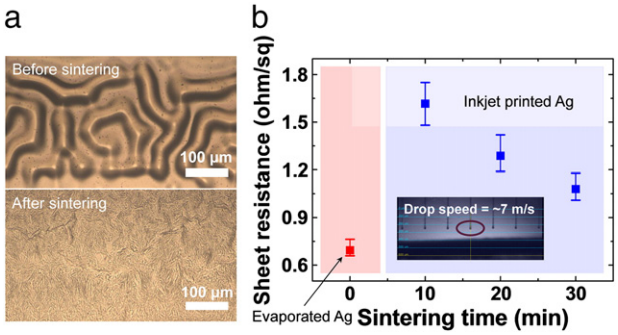

Fig. 2. (a) Optical microscopy images (20×) of an silver electrode immediately after inkjet printing, before sintering (upper image) and 30 min after sintering (lower image). (b) Sheet resistance of an inkjet-printed silver electrode after sintering times of 10, 20, and 30 min. The sheet resistance of thermally evaporated silver is also shown for comparison. The inset shows an optical capture image of a silver ink drop.

layer, and then dried overnight at room temperature in a N_2-filled glove box.

2.3. Self-assembled monolayer surface treatment

To form the OTS SAM on the SiO_2/Si substrate, the substrate was cleaned by a standard solvent cleaning process (using acetone followed by IPA and then DI water in an ultrasonic bath for 20 min) and dried with N_2 gas. The cleaned substrate was immersed in a prepared OTS solution (0.1 wt% in anhydrous toluene) for ~12 h in a glove box. Then, the modified substrate was cleaned again under running toluene and dried with N_2 gas.

3. Results and discussion

3.1. Electrical characteristics of TIPS pentacene OFETs

The electrical characteristics of the TIPS pentacene OFETs are summarized in Fig. 3. Figs. 3(a) and (b) show the transfer characteristics (drain current versus gate-source voltage) for a fixed drain-source voltage (V_{DS}) of −40 V. Figs. 3(c) and (d) show the output characteristics (drain current versus drain-source voltage) for different gate voltage (V_G) values. Figs. 3(a) and (c) correspond to untreated TIPS pentacene OFETs, whereas Figs. 3(b) and (d) correspond to the devices with rGO surface treatment. It is clear that the drain current increased by an order of magnitude due to the rGO surface treatment of the SiO_2 dielectric. Also, we found that the field effect mobility of the carriers increased from 0.082 $cm^2/V{\cdot}s$ to 0.141 $cm^2/V{\cdot}s$ due to the rGO surface treatment. The inset of Fig. 3(b) shows the electrical characteristic of devices coated with only rGO (i.e., without TIPS pentacene deposition). The reason of no conductivity with the rGO through the source and drain electrodes is because the grain size of rGO is much smaller than the channel length in our devices (see Fig. 1). There are many discontinuities between individual rGO grains. Therefore, the leakage conducting paths are blocked, which results in typical p-type FET characteristics by TIPS pentacene.

3.2. Enhanced performance of rGO-treated OFETs

The enhanced performance of rGO-treated OFETs can be explained by the effect of dielectric/channel surface properties on the morphology of the active TIPS pentacene layer. Figs. 4(a) and (b) show atomic force microscope (AFM) topological images of untreated and rGO-treated TIPS pentacene OFETs, respectively. Cross-sectional profiles are also shown, corresponding to cuts across the dashed lines in these images. The morphological grain size and vertical gradient of the TIPS pentacene layer for the rGO-treated TIPS pentacene OFETs are significantly larger than those of the untreated TIPS pentacene OFETs. This indicates a decrease in the number density of active channel grain boundaries. Thus, the number of interfacial trapping sites and the probability of carrier scattering was also reduced, resulting in a decrease in the total channel resistance and an increase in the mobility of the rGO-treated OFET devices [4,5]. We calculated the density of interfacial trapping sites (n_{trap}) using the following equation [32,33]:

$$n_{trap} = \frac{C}{q}\left(\frac{qSloge}{kT} - 1\right) \quad (1)$$

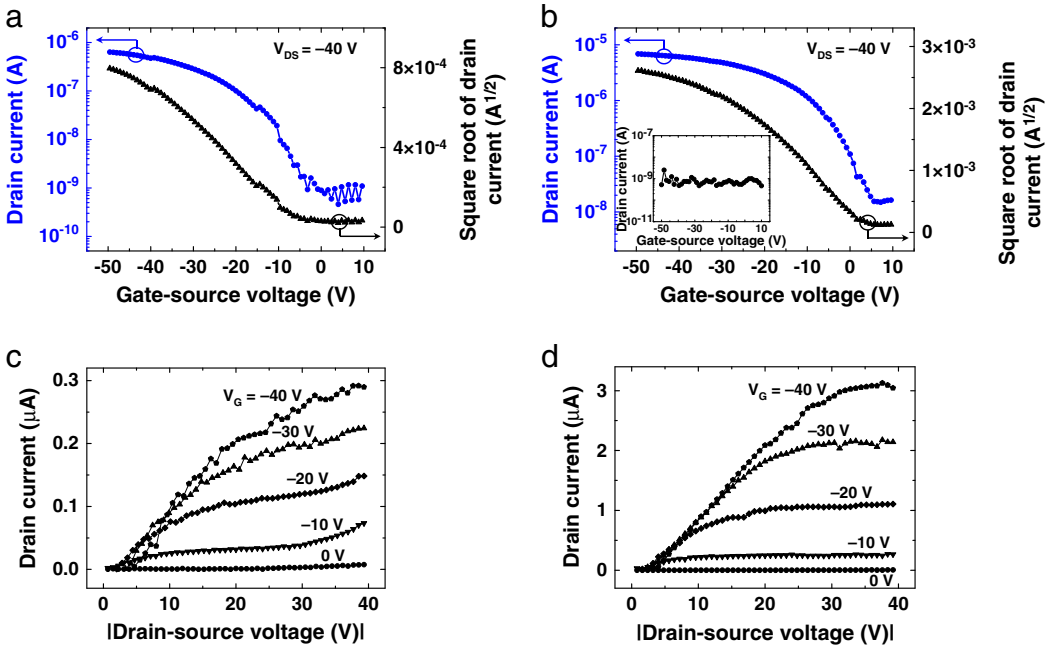

Fig. 3. Device characteristics of (a and c) untreated and (b and d) rGO-treated TIPS pentacene OFETs. (a and b) Drain current and square root of the drain current versus gate-source voltage at a fixed V_{DS} = −40 V. (c and d) Drain current versus drain-source voltage at different gate voltages. The inset in (b) shows data for rGO layer only, without TIPS pentacene.

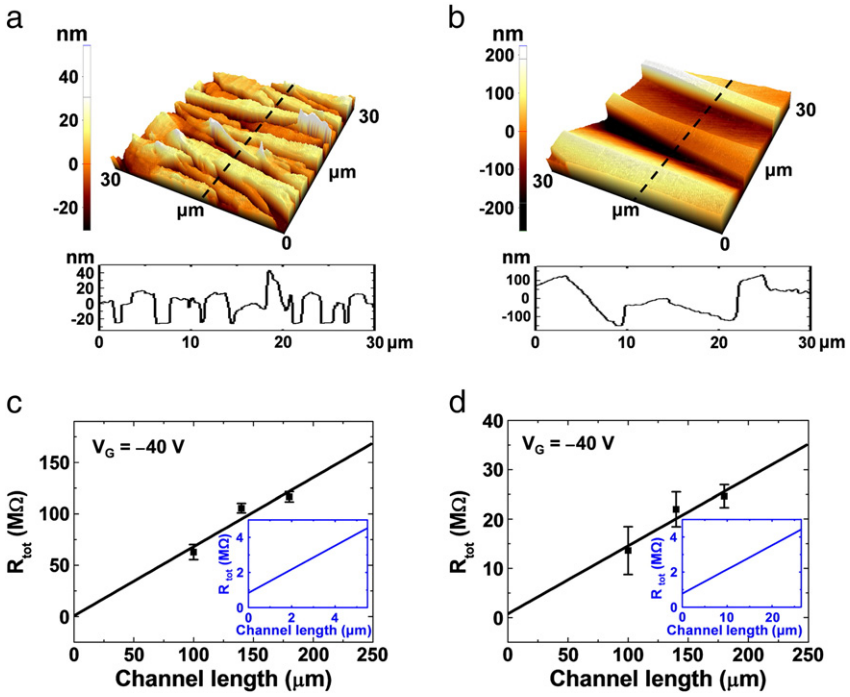

Fig. 4. AFM images (30 μm × 30 μm) with cross-sectional profiles of (a) an untreated TIPS pentacene layer and (b) a rGO-treated TIPS pentacene layer. Total resistance versus channel length for (c) untreated TIPS pentacene OFETs and (d) rGO-treated TIPS pentacene OFETs, at a fixed V_G of −40 V (saturation region). Inset plots are magnified at the *y*-intercept, showing similar contact resistances for the two cases.

where q is the elementary charge, S is the subthreshold swing, e is Euler's number, k is Boltzmann's constant, and T is the temperature. The results for the estimated n_{trap} and other parameters are summarized in Table 1. It can be observed that the interfacial trap density decreased from 1.84×10^{13} cm^{-2} to 1.33×10^{13} cm^{-2}, corresponding to a roughly 30% reduction from the original value.

Figs. 4(c) and (d) show the total resistance versus the channel length for untreated and rGO-treated TIPS pentacene OFETs, respectively, in the saturation region. As expected, the total resistance of untreated TIPS pentacene OFETs in the saturation region was significantly (roughly, five times) higher than that of the rGO-treated TIPS pentacene OFETs. In general, the contact resistance can be estimated by the transmission line method (TLM), in which the contact resistance is determined as the *y*-intercept of the extrapolation from the total resistance versus the channel length plot. However, if the output characteristics of the devices are nonlinear, it is not trivial to measure a constant total resistance from the initial slope at a low source-drain voltage range. In this case, the total resistance may be obtained from the saturation region instead of the low voltage region to estimate the contact resistance by modified TLM method [34].

We found that the contact resistance (*y*-intercept) was almost the same in both cases (approximately 1 MΩ), that is, the decrease of total resistance naturally means the decrease of channel resistance in the active layer. It is because the charge injection at the contact is determined by the electrode/channel interface while the rGO surface treatment affects the dielectric/channel interface only in terms of the transport efficiency of the channel region. The error bars in these figures were based on the standard deviation of 5–8 devices measured at each data point.

Table 1
Device performance parameters for TIPS pentacene OFETs on SiO_2, on rGO, and with OTS SAM.

	Mobility ($cm^2/V \cdot s$)	Threshold voltage (V)	I_{on}/I_{off}	Interfacial trap density (cm^{-2})
TIPS pentacene on SiO_2	0.082 ± 0.031	−12.7	2.56×10^3	1.84×10^{13}
TIPS pentacene on rGO	0.141 ± 0.049	−4.61	2.20×10^3	1.33×10^{13}
TIPS pentacene with OTS SAM	0.215 ± 0.060	−7.55	1.14×10^3	1.38×10^{13}

3.3. TIPS pentacene OFETs treated with OTS SAM

We also fabricated TIPS pentacene OFETs using an OTS SAM treatment, which is a widely used surface treatment method for OFETs on SiO_2/Si substrate [7,10]. Fig. 5(a) shows the transfer characteristics of the OTS SAM-treated TIPS pentacene OFETs, and Fig. 5(b) shows the channel-length dependence of the resistances of the devices. Compared with untreated TIPS pentacene OFETs (Figs. 3(a) and (c)), the OTS SAM-treated devices showed higher currents or lower resistances and higher mobilities (Table 1) due to the morphological improvements in the TIPS pentacene channel layer. The rGO surface treatment method has a very similar effect on the TIPS pentacene layer as the conventional OTS SAM treatment, in terms of the morphological enhancement of active layer and general transfer characteristics of the OFETs. Although it requires a long time to deposit SAMs on dielectric surface, this mixed structure containing rGO is simple to make and can be applied to various types of gate insulating materials other than SiO_2 dielectric to improve device performance.

4. Conclusions

We studied all solution-processed TIPS pentacene OFET devices in which the source and drain electrodes were patterned with inkjet-printed silver and dispersible rGO layer was deposited on the SiO_2/Si substrate as a surface treatment. All solution-processing techniques with inkjet printing made it possible to fabricate the devices easier and simpler than conventional manufacturing process of OFETs. The sheet resistance of the inkjet-patterned silver electrodes was comparable to that of evaporated silver electrodes. The rGO-treated OFETs exhibited improved device performance compared to untreated OFETs. The total resistance decreased dramatically for the rGO-treated OFETs, whereas the contact resistance was similar regardless of rGO treatment. The

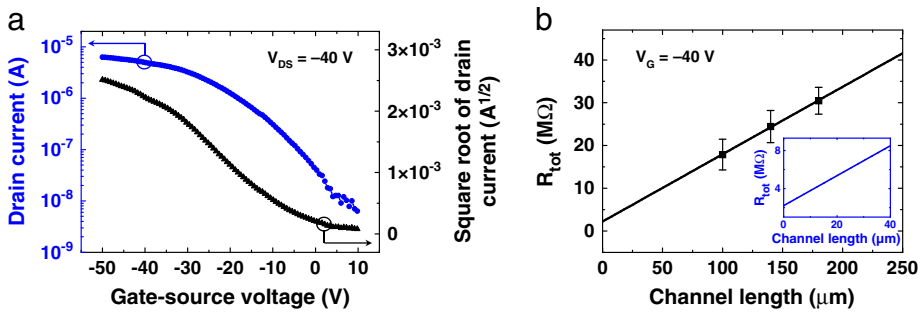

Fig. 5. Device characteristics of TIPS pentacene OFETs with OTS SAM treatment. (a) Drain current and square root of the drain current versus gate-source voltage at a fixed V_{DS} of −40 V. (b) Total resistance versus channel length at a fixed V_G of −40 V (saturation region).

field effect mobility improved from 0.082 $cm^2/V{\cdot}s$ to 0.141 $cm^2/V{\cdot}s$ following rGO treatment of the OFETs. We found that the improved electrical performance of OFETs was related to the enhanced morphological grain size with the decreased number of interfacial trapping sites. Although some non-uniformity and difficulties in patterning have been observed with solution-coated rGO, we can expect that the mixed structure containing rGO will be potentially applied to various types of substrates for device performance enhancement.

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