# Investigation of threshold voltage instability induced by gate bias stress in ZnO nanowire field effect transistors

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## Abstract
We investigated the threshold voltage instability induced by gate bias ($V_G$) stress in ZnO nanowire (NW) field effect transistors (FETs). By increasing the $V_G$ sweep ranges and repeatedly measuring the electrical characteristics of the ZnO NW FETs, the $V_G$ stress was produced in the dielectric layer underneath the ZnO NW. Consequently, the electrical conductance of the ZnO NW FETs decreased, and the threshold voltage shifted towards the positive $V_G$ direction. This threshold voltage instability induced by the $V_G$ stress is associated with the trapping of charges in the interface trap sites located in the ZnO NW–dielectric interface. Our study will be helpful for understanding the stability of ZnO NW FETs during repetitive operations.

(Some figures may appear in colour only in the online journal)

## 1. Introduction

ZnO nanomaterials have attracted considerable attention due to their direct wide band gap ($\sim$3.4 eV), large exciton binding energy ($\sim$60 meV), and potential use in various applications, such as field effect transistors (FETs), chemical and biological sensing, light-emitting devices, solar cells, and logic circuits [1–7]. Specifically, the use of one-dimensional ZnO nanowires (NWs), which have a large surface-to-volume ratio, is suitable for developing an understanding of the electronic transport properties that are influenced by the surrounding environmental factors, such as ambient gases ($O_2$, $N_2$, and water molecules) and other attached materials (core/shell structures and other thin films). For example, the adsorption and desorption of molecules can lead to the electron trapping–detrapping effect at the surface of the ZnO NW, which changes the depletion region in the NW channel [8–11]. The interfacial properties play an important

role in the performance characteristics of ZnO NW FETs. The interface-related electrical phenomena of ZnO NW FETs have been investigated under various environments using ZnO NW FETs [6–12]. For example, Li *et al* examined the properties of ZnO NW FETs by controlling the oxygen concentration in a vacuum chamber, which resulted in a change in the drain current and a shift in the threshold voltage [11]. We also examined the effects of passivation and the gate bias sweep rate on the characteristics of ZnO NW FETs under different environmental gases, including oxygen [9, 10]. When the gate bias time increased, more electrons were trapped on the ZnO NW surface by the adsorbed oxygen ions, which resulted in a reduction in the NW conduction channel [10]. However, the characteristics of ZnO NW FETs have not been thoroughly studied under repetitive operation of the gate bias.

In this study, we specifically investigated the interface-related phenomena of ZnO NW FETs induced by a gate bias ($V_G$) sweep stress. We applied the $V_G$ stress using
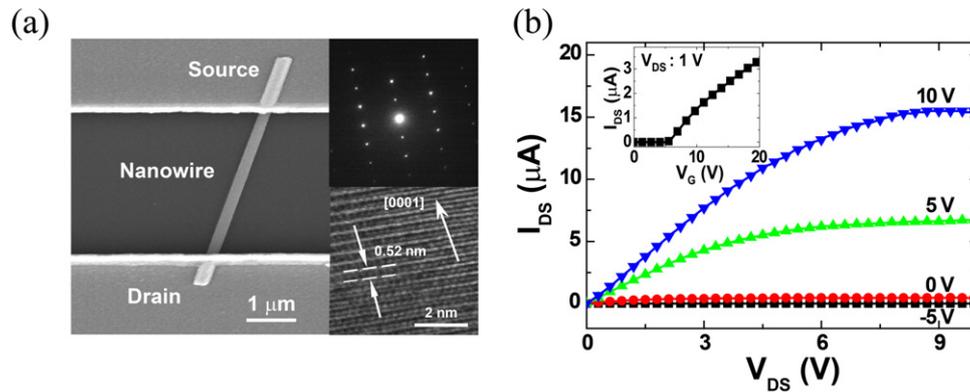
**Figure 1.** (a) FESEM image of a ZnO NW across the source and drain electrodes. The insets show an electron diffraction pattern (upper image) and a HRTEM image of a ZnO NW (lower image). (b) The representative $I_{DS}$−$V_{DS}$ curve of a ZnO NW FET and $I_{DS}$−$V_G$ (inset) before the $V_G$ stress was applied in the dark.

different sweep ranges to the bottom-gated ZnO NW FETs. We observed that the threshold voltage ($V_{th}$) shifted towards the positive $V_G$ direction when the $V_G$ stress was applied. This shift resulted because the $V_G$ stress increased the depletion width in the ZnO NW conducting channel due to the electrons trapped in the ZnO NW–gate dielectric interface. Our study will enhance the understanding of the interfacial properties and stability of ZnO NW devices during repetitive operations.

## 2. Experimental details

The ZnO NWs for this study were grown on an Au-coated *c*-plane sapphire substrate using ZnO and graphite powders with the carbothermal reduction process. The details concerning the growth of ZnO NWs have been previously reported [15]. To fabricate the ZnO NW FET devices, the ZnO NWs were dispersed in isopropyl alcohol by sonication to detach them from the sapphire substrate, and then they were dropped onto a silicon substrate, which was a 100 nm-thick layer of $SiO_2$ that was thermally grown on heavily doped p-type silicon to function as a bottom gate. Additionally, metal electrodes consisting of Ti/Au (30/50 nm) were deposited using an electron beam evaporator and defined as the source and drain electrodes using photolithography and the lift-off process. Figure 1(a) presents a field emission scanning electron microscopy (FESEM) image of a single ZnO NW FET device. The inset of figure 1(a) shows the high-resolution transmission electron microscopy (HRTEM) image (lower right image of figure 1(a)) and the corresponding electron diffraction pattern (upper right image of figure 1(a)) of this device. Finally, the fabricated ZnO NW FETs were passivated with poly(methyl methacrylate) (PMMA) to prevent the absorption of $O_2$ or water molecules [15]. The electrical properties of the ZnO NW FETs were systematically characterized as a function of the $V_G$ sweep range using a semiconductor parameter analyzer (Agilent B1500A) at room temperature with a probe system in the dark. The representative output characteristics (source–drain current versus source–drain bias, $I_{DS}$−$V_{DS}$) and transfer characteristics (source–drain current versus gate bias,

$I_{DS}$−$V_G$) of the ZnO NW FETs before the $V_G$ stress was applied are shown in figure 1(b) and the inset of figure 1(b), respectively. The $I_{DS}$−$V_G$ curve (figure 1(b)) indicates the ZnO NW FET's conventional enhancement-mode n-type characteristics, i.e., a zero off-current at zero $V_G$ and a positive $V_{th}$.

## 3. Results and discussion

### 3.1. Electrical properties of ZnO NW FETs with various $V_G$ sweep ranges

To analyze the electrical stability of the passivated ZnO NW FETs, the influence of the $V_G$ stress on the drain current through the NW channel was investigated. Figures 2(a)–(f) display a series of $I_{DS}$−$V_G$ curves measured at different $V_G$ sweep ranges (4, 10, 20, 30, 50, and 70 V) at a fixed drain bias ($V_{DS}$) of 1 V. The measurements of these $I_{DS}$−$V_G$ curves for each $V_G$ sweep range were repeated at least five times. After we first measured the electrical characteristics of the ZnO NW FET with a $V_G$ sweep range of 4 V, we waited for 1 h before we measured the device characteristics with the next $V_G$ sweep range of 10 V to prevent any decay behavior of the drain current in the ZnO NW FET [11–14]. Using the same procedure, we sequentially measured the electrical characteristics of the ZnO NW FET with $V_G$ sweep ranges of 20, 30, 50, and 70 V, waiting for 1 h after each measurement. Here, an interesting finding is that in the small $V_G$ sweep ranges (4, 10, 20, and 30 V), the change in the drain current was negligible, as shown in figures 2(a)–(d). However, in the large $V_G$ sweep ranges (50 and 70 V), the drain current of the ZnO NW FET gradually decreased during the measurements from the 1st cycle to the 5th cycle, as shown in figures 2(e) and (f). The reduction of the drain current is associated with the shift of $V_{th}$ to the positive $V_G$ direction. To more distinctly compare the $V_{th}$ shift of the ZnO NW FET for different $V_G$ sweep ranges, we plotted the $I_{DS}$−$V_G$ curves of the 5th cycle in figure 3(a) and those of the 1st cycle in the inset of figure 3(a).

The shift of the $V_{th}$ for different $V_G$ sweep ranges was not observed during the 1st measurement cycle, as shown in
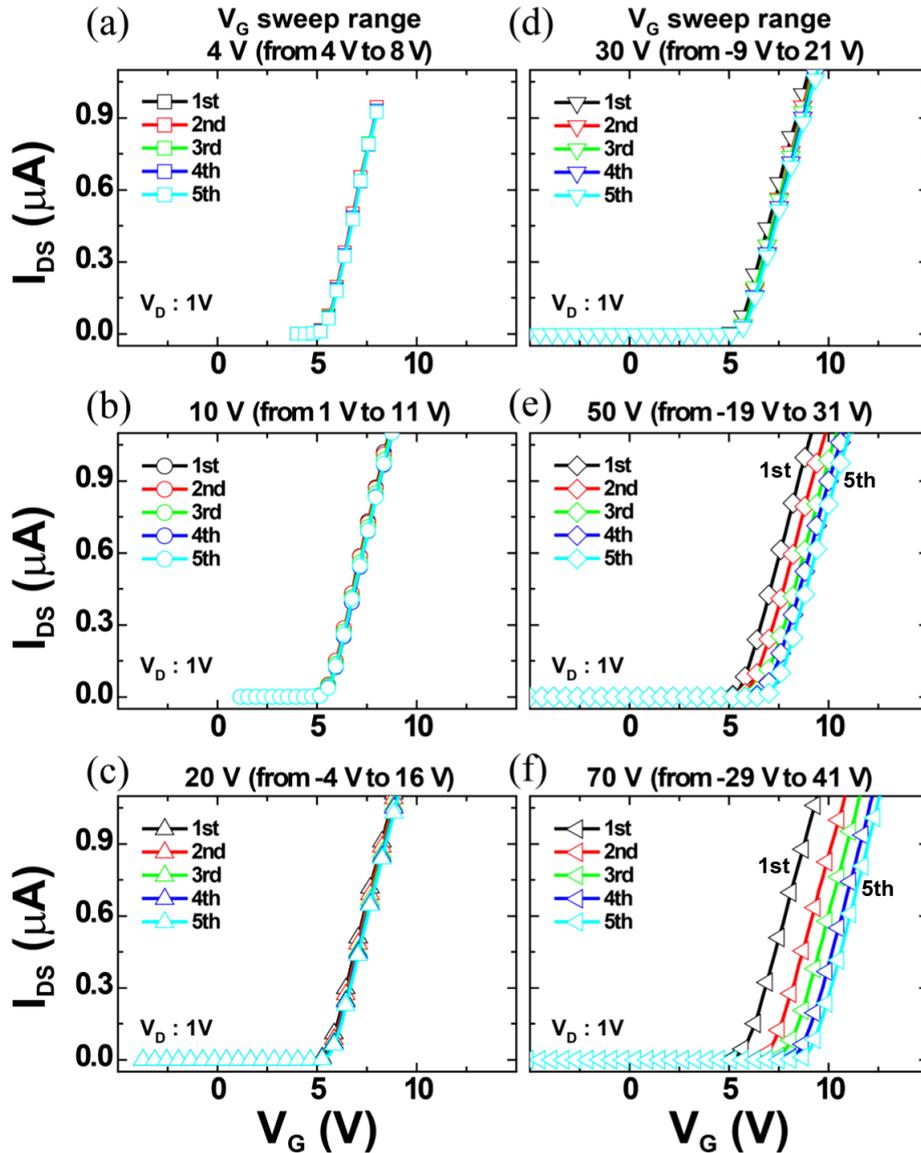
**Figure 2.** A series of $I_{DS}-V_G$ curves for a ZnO NW FET as a function of the $V_G$ sweep ranges of (a) 4 V (from 4 to 8 V), (b) 10 V (from 1 to 11 V), (c) 20 V (from −4 to 16 V), (d) 30 V (from −9 to 21 V), (e) 50 V (from −19 to 31 V), and (f) 70 V (from −29 to 41 V) at a fixed $V_{DS}$ of 1 V in the dark.
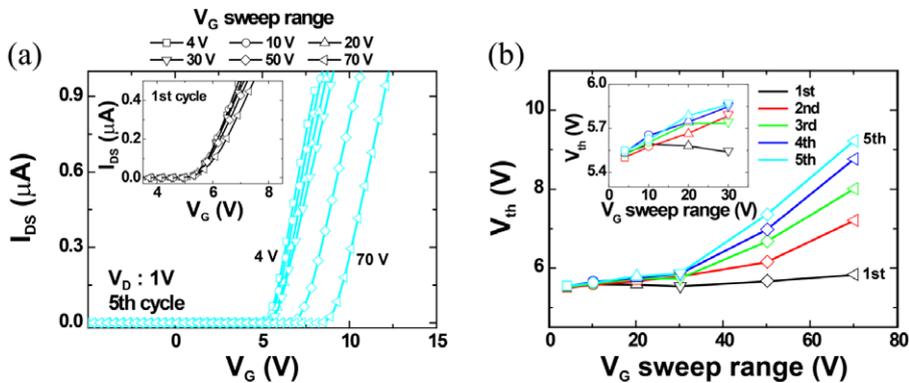


**Figure 3.** (a) The 5th measurement of the $I_{DS}-V_G$ curves for a ZnO NW FET with different $V_G$ sweep ranges (4, 10, 20, 30, 50, and 70 V) at a fixed $V_{DS}$ of 1 V. The inset shows the 1st measurement of the $I_{DS}-V_G$ curves for the same $V_G$ sweep ranges. (b) The $V_{th}$ as a function of the $V_G$ sweep ranges obtained from (a). The inset is a magnified plot near the $V_{th}$ of 5.7 V.
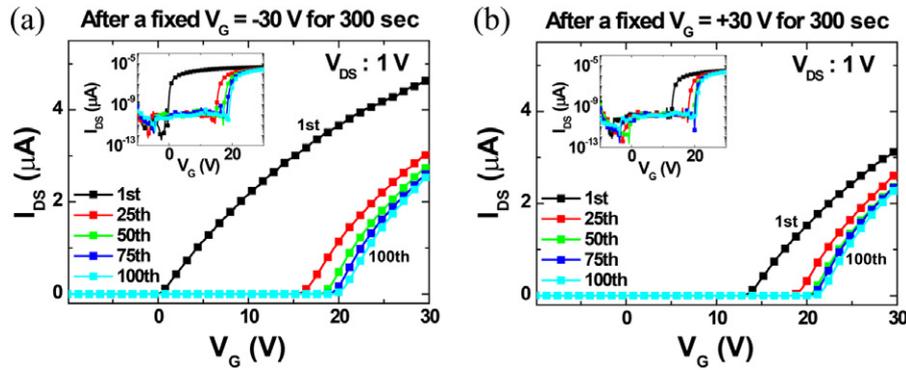
**Figure 4.** Repetitive 100-measurement cycles of $I_{DS}-V_G$ curves for a ZnO NW FET after maintaining a fixed $V_G$ of (a) $-30$ V and (b) 30 V for 300 s in the dark. The semi-logarithmic plots of $I_{DS}-V_G$ curves are shown in the insets.

the inset of figure 3(a). However, during the 5th measurement cycle, the $V_{th}$ clearly shifted towards the positive $V_G$ direction for the large $V_G$ sweep ranges (50 and 70 V), as shown in figure 3(a). These results can be explained by the $V_G$ stress effect, which has also been observed in thin film transistors (TFTs) [16–19]. Lee *et al* reported an experimental and modeling study of bias-stress-induced $V_{th}$ instability in amorphous indium–gallium–zinc oxide TFTs [16]. The shift of the $V_{th}$ towards the positive $V_G$ direction was attributed to the trapping of charges at or near the interface of the active channel and gate dielectric layers [16–19]. Figure 3(b) displays the $V_{th}$ of the ZnO NW FET as a function of the $V_G$ sweep ranges obtained from figure 3(a). The $V_{th}$ of the ZnO NW FET was determined by extrapolating the linear region of the maximum slope to the zero drain current; here, the point of maximum slope is the point where the transconductance ($g_m = dI_{DS}/dV_G$) is maximal [15]. The $V_{th}$ change was indeed negligible for the small $V_G$ sweep ranges (4, 10, 20, and 30 V). In these $V_G$ sweep ranges, the $V_{th}$ shift was observed to be less than 0.3 V. However, the $V_{th}$ dramatically shifted to the positive $V_G$ direction for the large $V_G$ sweep ranges (50 and 70 V). The $V_{th}$ shift for the $V_G$ sweep ranges of 50 and 70 V was observed to be 1.7 and 3.4 V, respectively. Similar to TFTs [16–19], the trap sites located at the ZnO NW–SiO$_2$ dielectric interface can capture the electrons from the ZnO NW, which increases the depletion width at the bottom of the ZnO NW and then partially screens the applied gate electric field. Therefore, when the large $V_G$ sweep range was applied to the gate dielectric layer, a larger and positive $V_G$ was required to flow the drain current through the ZnO NW channel because of the lowered effective $V_G$. A more detailed explanation is provided later by utilizing schematic energy band diagrams (figure 6).

### 3.2. $V_G$ stress effect on ZnO NW FETs by repetitive measurement conditions

We investigated the $V_G$ stress effect on the ZnO NW FETs by repeatedly measuring the $I_{DS}-V_G$ curves 100 times after maintaining a fixed $V_G$ of $-30$ V (figure 4(a)) and 30 V (figure 4(b)) for 300 s. Before applying the $V_G$ stress, the $V_{th}$ of the ZnO NW FET was 5.2 V (see figure 1(b)). After

maintaining a fixed $V_G$ of $-30$ V, the $V_{th}$ shifted to 0.2 V (figure 4(a), 1st curve) because the electrons that were trapped in the interface trap sites at the ZnO NW–SiO$_2$ interface were released and transferred to the ZnO NW by applying a $V_G$ of $-30$ V, which resulted in a reduction of the depletion width of the ZnO NW FET. Therefore, the electrical conductance of the ZnO NW FET increased, and the $V_{th}$ shifted towards the negative $V_G$ direction. When repeatedly measuring the $I_{DS}-V_G$ curves, the $V_G$ stress occurred in the dielectric layer, and the electrons in the NW channel were re-trapped in the interface trap sites at the ZnO NW–SiO$_2$ interface. Accordingly, the $V_{th}$ gradually shifted towards the positive $V_G$ direction and became saturated as the number of measurement cycles increased. In contrast, after maintaining a fixed positive $V_G$ of 30 V, the $V_{th}$ initially shifted to 12.4 V because the free electrons from the ZnO NW were trapped in the interface trap sites, which enlarged the depletion width of the ZnO NW FET. Consequently, the electrical conductance of the ZnO NW FET decreased, and the $V_{th}$ shifted towards the positive $V_G$ direction. Then, by increasing the number of measurement cycles, the $V_{th}$ also shifted towards the positive $V_G$ direction. A large number of trapped electrons in the interface trap enlarged the depletion width of the ZnO NW FET. When the $V_G$ stress was repeatedly applied, the concentration of electrons trapped in the ZnO NW–SiO$_2$ interface increased, which caused the depletion width to enlarge and the $V_{th}$ to shift.

To clearly show the $V_{th}$ shift of the ZnO NW FETs as a function of the $V_G$ measurement cycles after maintaining a fixed $V_G$ of either $-30$ or 30 V for 300 s, we extracted the individual $V_{th}$ values from the $I_{DS}-V_G$ curves at each cycle. As shown in figure 5(a), the $V_{th}$ constantly shifted to the positive $V_G$ direction due to the increased concentration of electrons trapped in the interface trap sites. When the number of measurement cycles was further increased, the $V_{th}$ saturated because there were no more trap sites being generated [17, 18]. Figure 5(b) displays the mobility and carrier density of the ZnO NW FET as a function of measurement cycles after maintaining a fixed $V_G$ of $-30$ and 30 V for 300 s. The mobility ($\mu$) and carrier density ($n_e$) of the ZnO NW FET can
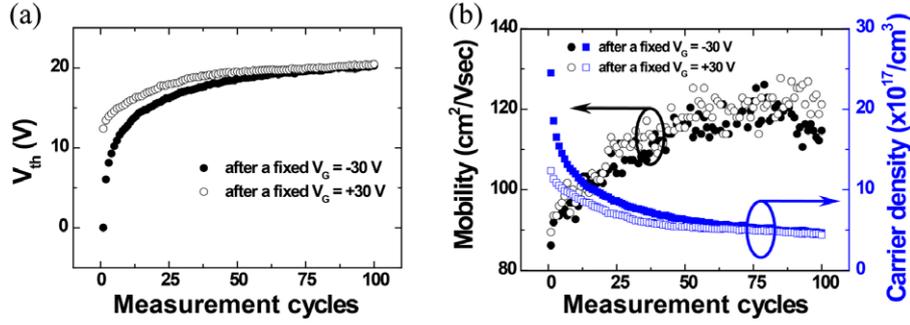
**Figure 5.** (a) The $V_{th}$ shift for the ZnO NW FET as a function of measurement cycles and (b) mobility and carrier density for the ZnO NW FET as a function of measurement cycles after maintaining a fixed $V_G$ of $-30$ and $30$ V for $300$ s.
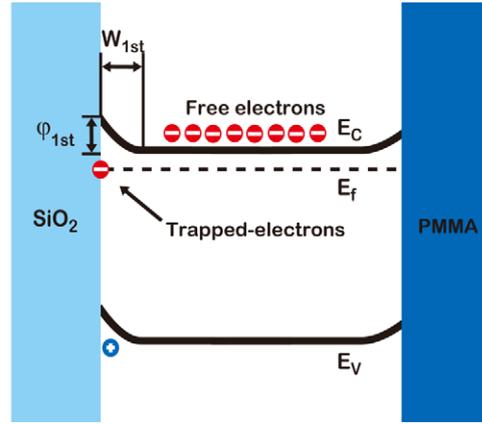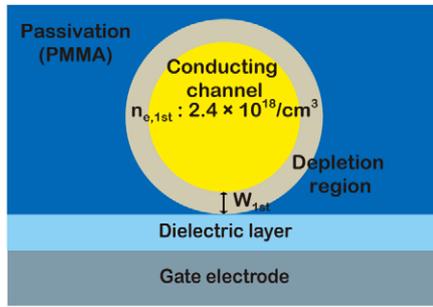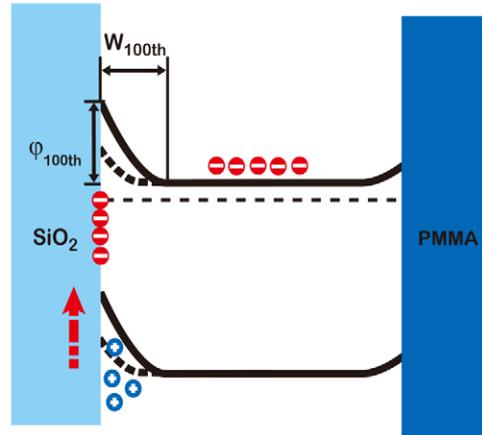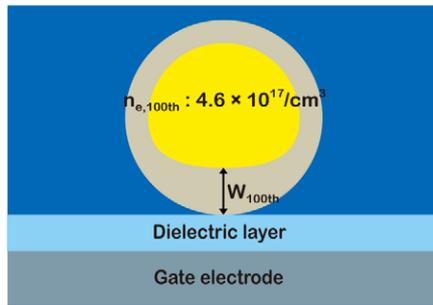


**Figure 6.** Schematic illustration of the cross-sectional views across the ZnO NW FET and their corresponding equilibrium energy band diagrams of (a) the 1st (initial state) measurement and (b) the 100th ($V_G$ stress state) measurement of the $I_{DS}$–$V_G$.

be calculated from equations (1) and (2), respectively [15].

$$\mu = \frac{g_m L^2}{V_{DS} C_G} \quad (1)$$

$$n_e = \frac{Q_{tot}}{e \pi r^2 L} \quad (2)$$

where $Q_{tot}$ is the total charge in the NW ($Q_{tot} = C_G |V_G - V_{th}|$) and $C_G$ is the gate capacitance, which can be estimated using the model of a cylinder on an infinite metal plate as $C_G = 2\pi \varepsilon_o \varepsilon_{SiO_2} L / \cosh^{-1}(1 + h/r)$; here, $r$ is the radius

of the NW ($\sim$100 nm), $L$ is the channel length of the NW ($\sim$3 $\mu$m), $h$ is the thickness of the SiO$_2$ layer ($\sim$100 nm), $\varepsilon_o$ is the permittivity of free space, and $\varepsilon_{SiO_2}$ is the dielectric constant of SiO$_2$ ($\sim$3.9). Although the electrons may not be uniformly distributed throughout the entire ZnO NW channel, the carrier density of the ZnO NW FET can be estimated by assuming a uniform distribution of electrons and at an arbitrarily chosen $V_G$ of 25 V. For the case of maintaining a fixed $V_G$ of $-30$ V, the carrier density and mobility of the ZnO NW FET were calculated to be $2.4 \times 10^{18}$ cm$^{-3}$ and $86.2$ cm$^2$ V$^{-1}$ s$^{-1}$ for the 1st cycle, $6.3 \times 10^{17}$ cm$^{-3}$ and

**Table 1.** Summary of the device performance parameters that were obtained from the $I_{DS}$–$V_G$ curves of the ZnO NW FETs after maintaining a fixed $V_G$ of −30 and 30 V for 300 s.

| | $V_G$ condition | $V_{th}$ (V) | $\mu$(cm$^2$ V$^{-1}$ s$^{-1}$) | $n_e$ (×10$^{17}$ cm$^{-3}$) at $V_G = 25$ V |
|---|---|---|---|---|
| −30 V | 1st | 0.0 | 86.2 | 24.5 |
| | 25th | 16.2 | 104.1 | 8.6 |
| | 50th | 18.6 | 116.3 | 6.3 |
| | 75th | 19.6 | 122.0 | 5.3 |
| | 100th | 20.3 | 114.7 | 4.6 |
| +30 V | 1st | 12.4 | 89.5 | 12.3 |
| | 25th | 18.0 | 110.6 | 6.9 |
| | 50th | 19.5 | 115.5 | 5.4 |
| | 75th | 19.9 | 120.4 | 5.0 |
| | 100th | 20.5 | 121.2 | 4.4 |

116.3 cm$^2$ V$^{-1}$ s$^{-1}$ for the 50th cycle, and 4.6 × 10$^{17}$ cm$^{-3}$ and 114.7 cm$^2$ V$^{-1}$ s$^{-1}$ for the 100th cycle, respectively. When the number of measurement cycles for obtaining the $I_{DS}$–$V_G$ curve was increased, the carrier density decreased because of the increased concentration of trapped electrons, and the mobility increased due to the reduced scattering of electrons [20]. The electronic parameters of the ZnO NW FET for the case of maintaining a fixed $V_G$ of −30 and 30 V are summarized in table 1.

### 3.3. Electrical transport mechanism of ZnO NW FETs under $V_G$ stress

Figure 6 shows schematic illustrations of the cross-sectional views across the ZnO NW FET and their corresponding energy band diagrams at the 1st measurement (figure 6(a)) and at the 100th measurement (figure 6(b)) by the $V_G$ stress. The depletion width from the surface band-bending at the interfaces between the ZnO NW and its surroundings should be considered individually. Because the ZnO NW was physically placed on the SiO$_2$ substrate and passivated with a PMMA layer, the depletion width and surface barrier potential are generally different at each interface, i.e., one is the NW–SiO$_2$ interface and the other is the NW–PMMA interface. Here, for a simple discussion, we assume that the depletion width and surface barrier potential near the NW–PMMA interface remain unchanged for different $V_G$ stresses with the same NW–PMMA interface trap density and uniform charge distribution in the ZnO NW. Furthermore, it is likely that the $V_G$ stress effect has a greater influence on the NW–SiO$_2$ interface. For the 1st measurement of the ZnO NW FET, which is the initial state, the electronic conduction ($E_C$) and valence ($E_V$) bands of the ZnO NW present a surface band-bending with a depletion width ($W_{1st}$) and barrier potential ($\varphi_{1st}$) at the NW–SiO$_2$ interface. In contrast, for the 100th measurement of the ZnO NW FET, which is the $V_G$ stress state, the electronic band displays a surface band-bending with a relatively larger depletion width ($W_{100th}$) and higher barrier potential ($\varphi_{100th}$) than those of the 1st measurement due to the increased concentration of trapped electrons induced by the $V_G$ stress. Therefore, in the $V_G$ stress state, a higher gate electric field is required to create the conducting channel in the ZnO NW. However, as shown

in the inset of figure 4(a), the subthreshold slope does not change after the ZnO NW FET has undergone the $V_G$ stress effect, which indicates that no additional electron trap sites at the interface of ZnO NW–SiO$_2$ were created. The larger depletion width ($W_{100th}$) is primarily due to more electrons trapped in the traps located at the ZnO NW–SiO$_2$ interface. These trapped electrons partially screen the applied electric field such that the effective gate electric field is reduced, which corresponds to the $V_{th}$ shift. When the $V_G$ is repeatedly swept from negative to positive values, in the negative $V_G$ values, the trapped electrons can be released, but a period of time is required for the stress to relax. Therefore, within a few seconds between the measurement cycles, the $V_G$ stress continually accumulated in the dielectric layer of the ZnO NW FETs. Consequently, the observed results indicate that the enhanced density of trapped electrons resulting from the $V_G$ stress is expected to play an important role in the change of the depletion width and the shift of the $V_{th}$ in the ZnO NW FET.

## 4. Conclusions

In summary, we investigated $V_{th}$ instability induced by the $V_G$ stress in ZnO NW FETs. Based on the transfer characteristics measured with various $V_G$ sweep ranges and repetitive $V_G$ sweep cycles, the charge trapping phenomenon was the primary cause of $V_{th}$ instability in the ZnO NW FETs. When the $V_G$ stress was applied to the ZnO NW FET, the conduction electrons in the ZnO NW were captured in the NW SiO$_2$ interface trap sites; these trapped electrons then enlarged the depletion width of the ZnO NW, which resulted in a reduction in the effective $V_G$ electric field. When $V_G$ stress was applied, the electronic conductance decreased, and the $V_{th}$ value gradually shifted towards the positive $V_G$ direction. Because the $V_{th}$ showed a strong dependence on the $V_G$ stress effect in the ZnO NW FETs, the interfacial properties at the ZnO NW–dielectric layer should be considered important when the ZnO NW FETs are practically used in devices.

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