Enhanced characteristics of pentacene field-effect transistors with graphene electrodes and substrate treatments

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Pentacene organic field-effect transistors (OFETs) were fabricated with multilayer graphene films as the source and drain electrodes. The electrical properties of graphene electrode OFETs were monitored as the fabrication conditions were varied with surface treatments on the dielectric layer and substrate. With surface treatments, the performance of the graphene-electrode pentacene OFETs were significantly enhanced; the output currents increased by more than tenfold, and the mobility increased to levels as high as 1.2 cm^2/V s. Our results may foster the wide application of graphene electrodes in OFETs and other types of organic electronic devices. © *2011 American Institute of Physics*. [doi:10.1063/1.3629994]

Organic field-effect transistors (OFETs) have generated a great deal of research interest because of their low-cost fabrication, material variety, flexibility, and wide span of potential applications.[1,2] However, for practical applications, it is still crucial to improve the performance of the OFETs. To generate performance improvements, two research efforts have been implemented: (1) identifying the optimal electrode material for efficient charge injection to the active layers[3,4] and (2) improving the grain size and organization of the active organic semiconductor channel for efficient charge transport.[5,6] For example, to improve the grain size and molecular arrangement of the organic semiconductor channel, techniques such as high-temperature deposition of organic materials and dielectric-surface treatments with self-assembled monolayers of materials such as octadecyltrichlorosilane have shown promising results.[7,8]

Recently, graphene has received much attention as a promising electrode material for organic electronic devices.[3,4,9] In particular, multilayer graphene electrodes have been found to have low contact resistance due to a lower charge-injection barrier to the pentacene active layer in OFETs compared with the traditional Au electrode, as reported in our previous study.[9] Therefore, it can be expected that combining the efficient charge injection with graphene electrode and the easy charge transport from the high ordering of the organic channel can enhance the performance of the OFETs. However, such a combination has not yet been systematically investigated.

In this paper, the performance enhancement of pentacene organic field-effect transistors (OFETs) with multilayer graphene films as bottom-contact electrodes was investigated. Surface treatments were implemented to improve the molecular arrangement and the grains of the organic channel material during device fabrication. Using surface treatments, the electrical performance of pentacene OFETs with graphene electrodes was improved in terms of decreased channel resistances and increased mobility.

Figures 1(a) and 1(b) show the typical bottom-contact electrode device structure of the pentacene OFET used in our study. Transistors were fabricated on a heavily doped Si wafer, which serves as a common back-gate electrode. A SiO_2 layer with a 300 nm thickness was used as the gate dielectric. We used a multilayer graphene (MLG) film as the source and drain electrodes instead of a traditional metal electrode material, such as Au. The MLG film was grown by chemical vapor deposition (CVD) on nickel films. The grown MLG film was transferred and patterned into electrodes. The channel length and width of our pentacene OFETs were 100 μm and 1 mm, respectively. Then, 60-nm-thick

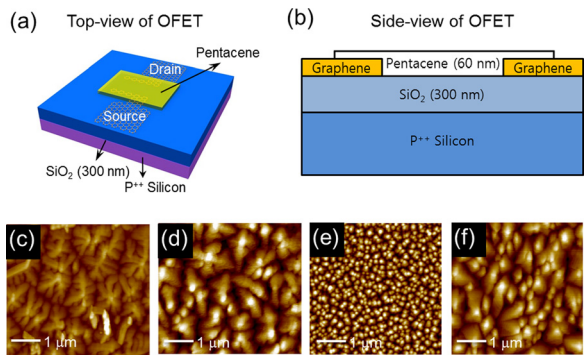

FIG. 1. (Color online) (a, b) Schematic of a bottom-gate graphene-electrode pentacene OFET: tilted top view (a) and side view (b). (c-f) AFM images (5 μm × 5 μm) of 60-nm-thick pentacene films deposited by organic vapor deposition onto 300-nm-thick SiO_2 under various conditions. (c) With no treatment, (d) pentacene deposition at 343 K, (e) OTS SAM treatment on the SiO_2 dielectric, and (f) pentacene deposition at 343 K and OTS SAM treatment on the SiO_2 dielectric.

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pentacene was deposited on top of the MLG electrodes and the dielectric layer at a rate of 0.2 Å/s by vacuum thermal evaporation. The pentacene was used as received (from Sigma Aldrich) without further purification. To investigate the effect of the surface treatment on the dielectric layer, we deposited an octadecyltrichlorosilane (OTS) self-assembled monolayer (SAM) on the SiO_2 layer by immersing the substrate in a silane solution (0.1 wt. %) in anhydrous toluene for ~12 h under a N_2 atmosphere. Subsequently, the modified substrates were cleaned in toluene for 20 min and then blow-dried with nitrogen gas. The details of the MLG growth and OFET device fabrication have been reported elsewhere.[9]

The morphology of the active layer, which can be controlled by varying the deposition conditions and the surface properties of the dielectric layer, affects the electrical characteristics.[7] Therefore, we studied the morphology of the pentacene films under various deposition conditions using an atomic force microscope (XE-100, Parks Systems, Inc.). The results are summarized in Figs. 1(c)–1(f). When the pentacene was deposited under standard conditions, without any variation of the deposition conditions, it showed a typical dendrite structure of pentacene grains (Fig. 1(c)). When the substrate temperature was increased to 343 K during the deposition, the grain size markedly increased, and the number of grain boundaries decreased, as seen when comparing Fig. 1(d) with Fig. 1(c). A decreased number of grain boundaries means that the probability of charge carrier scattering is reduced, therefore decreasing the channel resistance of pentacene active layer in OFETs.[10]

Furthermore, we deposited an OTS SAM on the dielectric surface prior to pentacene deposition. The OTS SAM is known to reduce the trapping interface states and to minimize the effect of dielectric polar functional groups.[11,12] The morphology of pentacene after the OTS SAM treatment exhibited no more dendrites, while the grain packing significantly increased with decreased grain size (Fig. 1(e)).[7] As a result, the contact property among the individual grains is known to be improved with decreased charge-trap states.[5,13] Ultimately, when the substrate temperature was raised to 343 K during the deposition and the substrate was pretreated with the OTS SAM, the grain size increased, as seen when comparing Fig. 1(f) with Fig. 1(e). With improved grain packing and larger grain size, this deposition condition enhanced the performance of OFETs to the highest level among all the conditions tested in this study.

Figure 2 summarizes a series of current-voltage characteristics of the graphene-electrode OFETs with pentacene deposited under the various aforementioned conditions: pentacene OFETs with graphene electrodes (denoted as type A, see also Fig. 1(c)), OFETs with pentacene deposited at a raised surface temperature of 343 K (type B, Fig. 1(d)), OFETs with OTS pretreatment on a SiO_2 dielectric (type C, Fig. 1(e)), and OFETs constructed using both conditions, i.e., pentacene deposited at 343 K and OTS treatment on SiO_2 dielectric (type D, Fig. 1(f)). Figure 2(a) shows the output characteristics (drain current versus drain voltage, I_D–V_D) for the representative devices of these four types at a various gate voltages (V_G) from 0 to −50 V at 10 V intervals. Figure 2(b) shows the transfer characteristics (drain current versus gate voltage, I_D–V_G) at a fixed drain voltage of −50 V. A photograph of a fabricated graphene-pentacene OFET device is shown in the inset of Fig. 2(a). The electrical characteristics for all the devices showed typical p-type OFET behavior. It can be seen that the charge transport characteristics were noticeably improved with pentacene deposition at a raised temperature (343 K) or with OTS treatment on the dielectric. In particular, when both treatments were used, the best performance was obtained from among the device types fabricated in this study. In the type-D devices, the saturation current reached ~170 μA, which was more than ten times larger than that of type-A devices (~15μA). This enhancement is originated from the morphology improvements of the pentacene films (Fig. 1) and subsequent decrease of the channel resistance, as we discussed above.

To analyze the device performance in more detail, we estimated the interfacial trap density (N_{trap}^{max}) using the following equation:[5,11]

$$N_{trap}^{max} = \frac{C}{q}\left[\frac{qS\log e}{k_B T} - 1\right] \quad (1)$$

where C is the capacitance of the gate insulator, q is the elementary charge, S is the subthreshold swing (SS) in V/decade, e (~2.718) is Euler's number, k_B is Boltzmann's constant, and T is the temperature.

According to Eq. (1), the type-D device shown in Fig. 2 yielded the lowest interfacial trap density of 1.91×10^{12} cm^{-2} among all of the device types because of the tighter packing of larger grains, which resulted in improved grain contact properties and reduced charge carrier scattering[10,14,15] compared with the other device types. On the other hand, the type-A device shown in Fig. 2 yielded the highest interfacial trap density of 5.11×10^{12} cm^{-2}.

Figure 2(b) shows the plots of the square root of I_D versus V_G at a fixed V_D of −50 V. The type-D devices displayed the highest current level compared to other devices. In addition, the on/off ratio of the type-D devices increased because of the increase of the on-current (I_{on}). These electrical parameters for the four types of devices are summarized in Table I.

Figure 3(a) displays the resistance values that were extracted from the linear regions in the output characteristics (V_D values from 0 to −1 V) for four types of devices as a

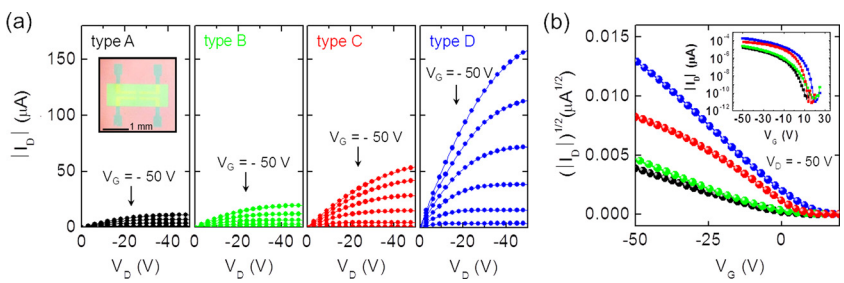

FIG. 2. (Color online) (a) I_D–V_D characteristics of the four types of graphene-electrode pentacene OFETs. The device types are marked in the plots. The inset shows a photograph of a fabricated OFET device. (b) I_D–V_G characteristics of the four types of graphene-electrode pentacene OFETs. The inset in (b) is plotted on a semilogarithmic scale.

TABLE I. Electrical characteristics of the graphene-electrode pentacene OFETs. T_S = substrate temperature, μ_{sat} = saturation mobility, V_{th} = threshold voltage, SS = subthreshold swing, $I_{on/off}$ = drain current on/off ratio, and N_{trap}^{max} = maximum interfacial trap density.

Device	Substrate	T_S(K)	μ_{sat} (cm^2/Vs)	V_{th} (V)	SS (V/dec)	$I_{on/off}$	N_{trap}^{max} ($\times 10^{12}$ cm^{-2})
Type A	SiO_2	300	0.01 ± 0.001	−9.18	3.91	10^6	5.11
Type B	SiO_2	343	0.18 ± 0.04	−6.53	4.02	10^6	4.16
Type C	OTS-SiO_2	300	0.58 ± 0.14	−4.97	1.79	10^7	2.30
Type D	OTS-SiO_2	343	0.94 ± 0.13	−3.38	1.88	10^7	1.91

function of the gate voltage. Here, the error bars were determined from the measurements of 5–7 devices for each type. These resistance values are the sum of the channel resistance and the contact resistance. We checked the contact resistance of the type A and type D devices using the transfer line method, and their values were found to be similar ~0.5 MΩ, indicating that the change of the resistance values is mainly due to the change of the channel resistances. Note that our evaluation of the contact resistance using the transfer line method may underestimate the contact resistance which may contain the channel length-dependent contact resistance term.[16–18] The reduction of the resistances of the type-D devices shown in Fig. 3(a) is in agreement with the morphological improvements shown in Fig. 1(f). That is, the improvements of the organic film morphology due to the high-temperature deposition or the dielectric surface treatment reduced the channel resistance.

The mobility of the OFETs was also significantly improved with surface treatments. Figure 3(b) shows the saturation mobility (μ_{sat}) of all the device types. In the saturation regime, the field-effect mobility can be calculated by the following equation:[17,19]

$$\mu_{sat} = \frac{2L}{WC}\left(\frac{\delta\sqrt{I_D}}{\delta V_D}\right)^2 \quad (2)$$

where W and L are the channel width and channel length, respectively. As shown in Fig. 3(b), the μ_{sat} is sequentially increased from 0.01 ± 0.001 cm^2/V s for the type-A devices, to 0.18 ± 0.04 cm^2/V s (type B), to 0.58 ± 0.14 cm^2/V s (type C), and ultimately to 0.99 ± 0.11 cm^2/V s in the type-D devices. The mobility of 0.99 cm^2/V s belongs in the range of the highest values that were achieved in the bottom-contact structure pentacene OFETs.[20] Moreover, the maximum mobility that we observed was 1.2 cm^2/V s in one of the type-D devices. In OFETs, the induced resistance from the interface of the electrodes with the semiconductor disturbed the charge injection and the induced high trap-density sites at the interface between the semiconductor and the insulator, hindering efficient charge flow.[12] Therefore, the relatively high mobility obtained in our pentacene OFET devices originated from the ordered pentacene morphology from surface treatments while the use graphene as an alternative electrode ensured good contact properties.

In conclusion, we demonstrated that the performance of pentacene OFETs could be improved significantly by combining the use of graphene electrodes and dielectric surface treatments. We showed that as the pentacene film morphology was improved with various dielectric surface treatments, the electrical performance of the graphene-electrode pentacene OFETs was also improved accordingly in terms of low threshold voltage, low subthreshold slope, large on/off ratio, and high field-effect mobility. Our results suggest that the use of various surface-treatment techniques brings synergetic improvements for high-performance OFETs with graphene electrodes and therefore may foster the wide application of graphene electrodes in other organic electronic devices.

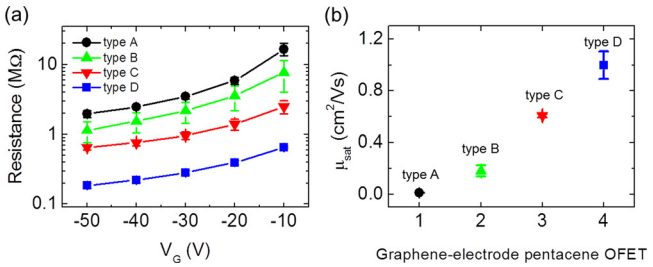

FIG. 3. (Color online) (a) The resistances and (b) saturation mobility (μ_{sat}) of the four different types of devices at various gate voltages. The error bars shown in the plots were obtained from the standard deviation of the measurements of 5–7 devices for each device type.

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