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Electrical Characterization of Unipolar Organic Resistive Memory Devices Scaled Down by a Direct Metal-Transfer Method

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Organic-based resistive memory has been considered to be a promising alternative to conventional semiconductor-based nonvolatile memories due to a variety of advantages such as low production cost, printability, simple fabrication and good scalability.[1–5] Organic-memory research to date has focused mainly on developing new organic materials or optimizing device structures.[6–10] However, the essential step for a more practical application of organic memories is to integrate as many memory cells into a single chip as possible. Organic resistive memory devices can be usually integrated into a patterned array, in which two electrodes are cross-aligned.[11] However, the fabrication of array-type organic memory devices with nanometer-scale junctions is not trivial. For example, the minimum feature size in patterned-array fabrication using shadow masks is limited to approximately 50 μm. Another problem with the use of conventional lithography techniques for organic semiconductors is that they are usually accompanied by a solution process for developing or removing the photoresist, which would dissolve an organic active layer previously coated onto the substrate. Alternative patterning techniques for organic-based memory devices, such as microcontact printing (μCP), nanoscale transfer printing (nTP), metal-transfer printing, and cold welding, have been actively studied.[12–15] However, there are several technical limitations to these fabrication processes. For example, μCP requires additional processes associated with the transfer of self-assembled monolayer (SAM) ink, such as the use of an etching mask.[16] Also, the SAM ink can spread laterally in and around the edges of the contact region, making it difficult to control pattern resolution. And, nTP and cold welding both require high pressures of over 300 MPa during the metal-transfer process[13,15] which would damage the organic active layer, and the transferred metal lines could also be deformed.

An alternative method potentially avoiding these technical drawbacks, the direct metal-transfer (DMT) method, has been introduced for the patterning of organic-based electronic devices.[17] DMT is a nonaqueous process used to transfer metal patterns from a stamp directly onto a substrate at a low temperature and pressure (100 °C and 2 MPa). This method can minimize the damage to the organic layer and enable three-dimensionally

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stackable device applications. DMT is also cost effective because the hard glass stamp is semipermanently used in repeatable transfer processes. Furthermore, the conformal contact between the hard glass stamp and the substrate usually yields a precisely shaped transferred pattern, leading to stable and reliable electrical characteristics in the fabricated devices.

In this study, we fabricated unipolar organic resistive memory devices in an 8×8 cross-bar array structure utilizing a nonaqueous DMT method for patterning the electrodes. Using this simple method, memory devices with a 2 μm junction size were fabricated, exhibiting a high ON/OFF ratio and stable switching characteristics. The memory parameters were studied statistically using the distribution of ON and OFF states and set threshold voltages. The devices also showed good memory performance in terms of memory endurance and retention characteristics. Finally, organic memory devices with a 100 nm junction size were also fabricated with the DMT method to demonstrate the feasibility of this technique in highly integrated nanoscale device applications.

Figure 1 shows the fabrication process of the organic memory devices in an 8×8 array structure with a cell size of 2 μm. The DMT method was used to minimize the damage to the organic layer and maximize the integration density. A stamp with a 2 μm line width was fabricated using conventional photolithography (Figure 1a), and then coated with a releasing material, providing a (tridecafluoro-1,1,2,2-tetrahydroctyltrichlosilane)-coated stamp (Figure 1b), followed by the deposition of Au. This molecular treatment of the stamp was necessary to facilitate the easy transfer of the Au metal from the stamp onto the organic layer. Patterned bottom electrode lines (Al) were next formed on an Si/SiO$_2$ substrate using photolithography (Figure 1c). A composite material consisting of polyimide (PI) and 6-phenyl-C61 butyric acid methyl ester (PCBM) was then prepared (refer to the Experimental section for details). PI has an excellent thermal stability and a high chemical resistance, allowing for reliable switching properties in ambient or even harsh conditions.[18,19] The PI:PCBM composite solution was then spin-coated onto the substrate (Figure 1d). The transparent glass stamp bearing the Au top electrodes was vertically aligned with the substrate coated with the organic active layer, and then a pressure of ~2.2 MPa was applied at an elevated temperature of ~100 °C to ensure conformal contact between the Au top electrode lines and the substrate (Figure 1e). Finally, the stamp was detached from the substrate (Figure 1f) to yield organic memory devices (Al/PI:PCBM/Au) fabricated in an 8×8 array structure (Figure 1g). In the case of the organic memory devices with a 100-nm cell size, the bottom electrodes were prepared on the substrate by nanoimprint lithography, and the top electrodes

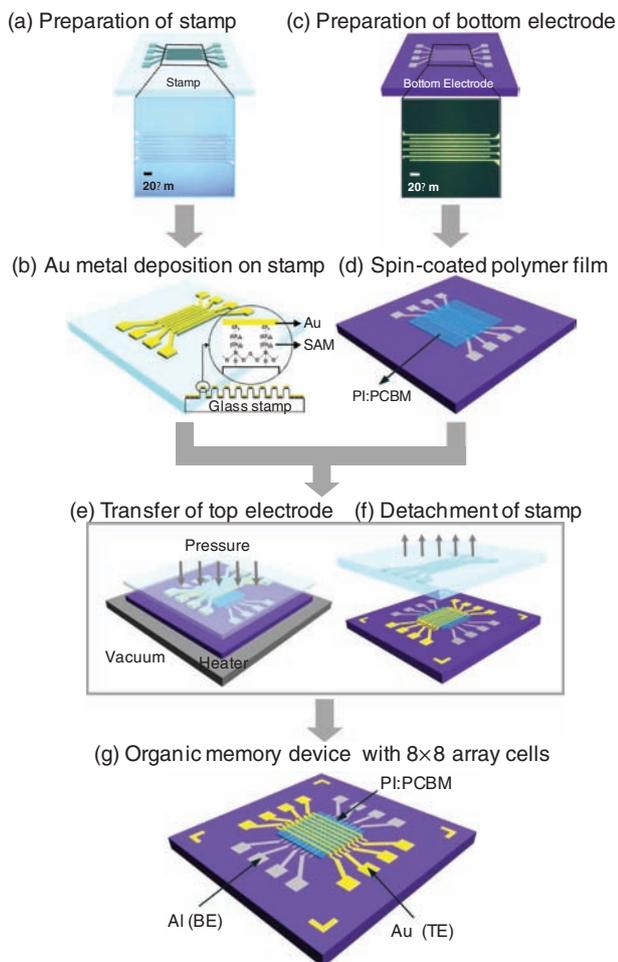**Figure 1.** Process flow of organic memory devices in an 8 × 8 structure using DMT. (a) Stamp with 2 μm-wide line patterns prepared using photolithography. (b) Deposition of Au film on the stamp coated with a releasing material. (c) Bottom electrodes with a 2 μm line width prepared using photolithography. (d) Spin-coated polymer film (PI:PCBM) onto the patterned bottom electrodes. (e) Transfer of the top electrodes from the stamp onto the substrate using DMT. (f) Detachment of stamp from the substrate. (g) Completed organic memory devices (Al/PI:PCBM/Au) in an 8 × 8 array.

were defined using DMT with a transparent stamp duplicated from a silicon master patterned by electron-beam lithography.

Figure 2a is an optical image of the 8 × 8 organic memory array (2 μm cells). An enlarged optical image is shown in the inset of Figure 2a. The top metal lines were transferred without any disconnections. The organic active film was then examined using cross-sectional transmission electron microscopy (TEM) (Figure 2b), revealing the stacked Al/PI:PCBM/Au structure. The thickness of the organic layer was measured at ~10 nm and the metal-transfer process did not cause any significant damage to the organic film.

The current–voltage (I–V) characteristics of the organic memory device are shown in Figure 2c. Voltage was applied to the Au top electrodes while the Al bottom electrodes were grounded. In the first double-sweep mode from 0 to 5 V and back to 0 V, the device showed an abrupt resistance change

when going from a high-resistance state (HRS; OFF state) to a low-resistance state (LRS; ON state) at a threshold voltage; this is called the memory-writing process. The LRS was stably maintained in the low-voltage range during the second (single) sweep, exhibiting a nonvolatile memory effect. When a voltage over ~4 V was applied to the device, the resistance state changed back to HRS; this is called the memory-erasing process. The device followed the same I–V curves in sequential sweeps (from the third to the sixth sweeps), exhibiting reproducible switching characteristics. These resistive switching phenomena may be associated with the charge-trapping/detrapping mechanism firstly introduced by Simmons and Verderber[20] and then extended by Bozano et al.[8,21] This model suggests that metal nanoparticles or small molecules embedded within the polymer matrix play an important role for the bistable switching effect. We also noticed that reproducible switching can be achieved by the oxide layer on the bottom Al electrodes.[22,23] It indicates the significance of selecting electrodes in our organic memory devices.

In particular, our organic resistive memory exhibited so-called "unipolar switching" behavior, in which switching to the ON and OFF states is achieved by applying different voltages with the same polarity.[24] In contrast, "bipolar switching" memory devices require both polarity voltages (positive and negative) to control the ON and OFF states.[25] Unipolar memory switching is an important trait in most practical device applications. Considering that a diode component should be added to each memory element to prevent cross-talk interference in array-type device structures, electrically rewritable cells in a one diode and one resistor ("1D-1R") architecture can be elaborated only by the use of unipolar switching memory devices.[26] The external circuit required for practical memory applications can also be simplified due to the use of a single voltage polarity. Meanwhile, the single storage medium of phase-separated semiconductor:ferroelectric polymer blend demonstrated a rectifying bistable resistive switch,[27] which can be considered to be an ultimate solution for solving the cross-talk problem.

Cell-to-cell uniformity is considered to be an important quality factor in memory devices. Figure 2d shows the statistical distribution of the ON and OFF currents of "working" cells (cells showing an ON/OFF ratio of over 10^3) in the 8 × 8 memory arrays. Both ON and OFF currents were read at 0.5 V. We found that the yield of the memory devices was 78% (50 out of 64 cells). Switching failure in some cells seems to be attributed to the existence of non-uniform film thickness locally. Although each ON and OFF state was distributed over a wide current range of approximately two orders of magnitude, the important point is that the ON states were well separated from the OFF states, indicating the memory margin was sufficient to distinguish each state. The inset of Figure 2d shows the histogram of the set threshold voltage (the voltage required to switch from the OFF state to the ON state). The set voltages ranged from 2.5 to 4.5 V.

Essential memory performance properties are characterized by the endurance and retention characteristics. To evaluate the performance of our organic memory device, we performed an endurance cycling test in DC sweeping mode. Each current state, read at 0.6 V, remained stable over 200 cycles, as shown in **Figure 3**a. Although some variation in each current state was
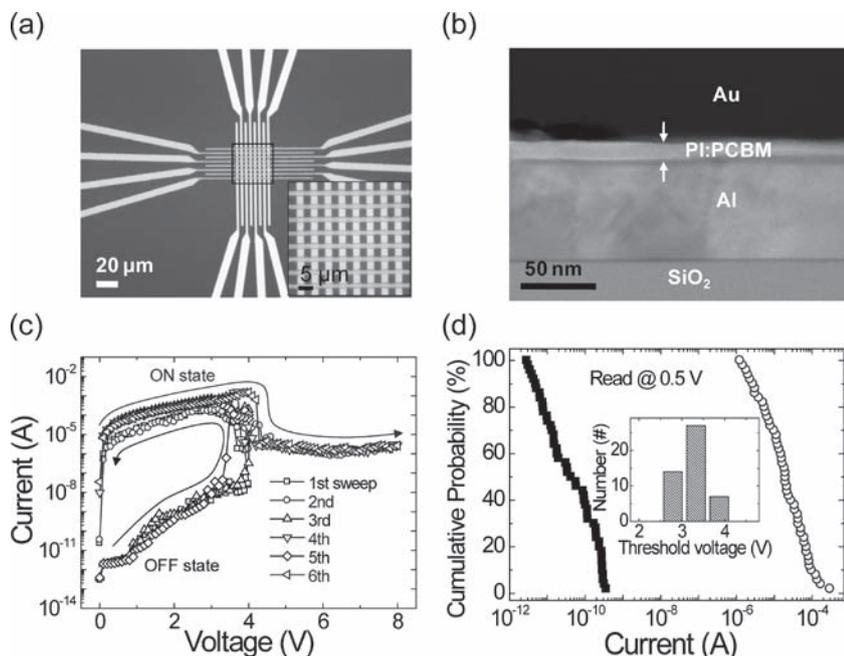
Figure 2. (a) An optical image of the organic memory devices in a 2 μm-scale 8 × 8 array structure. The inset image shows an overview of the entire area of the memory cells. (b) Cross-sectional TEM image of a 2 μm-scale organic memory device (Al/PI:PCBM/Au). (c) I–V characteristics of a 2 μm-scale organic memory device. (d) The cumulative probability data of operating cells in the 2 μm-scale organic memory devices. Fifty cells out of the 64 cells fabricated operated well (a yield of ~78%). The inset graph shows a histogram illustrating the statistical distribution of threshold voltages.

observed, the memory device constantly maintained a high ON/OFF ratio of over 10^3. We also measured retention performance to investigate the information storage ability of our organic memory devices. As shown in Figure 3b, the organic memory device showed a long retention of 10^4 s without serious electrical degradation. The high ON/OFF ratio of over 10^5 also remained stable during the retention test.

We also fabricated organic memory devices with a cell size of 100 nm in the 8 × 8 cross-bar structure, as shown in **Figure 4**a. These devices had 100 nm-wide bottom electrodes fabricated by nanoimprint lithography overlaid with crossed 100 nm-wide top electrodes produced using DMT. In this case, the patterns on the stamp were fabricated by electron-beam lithography, with a half-pitch of 100 nm. We used PI and PCBM concentrations somewhat different from those used for the 2 μm-scale
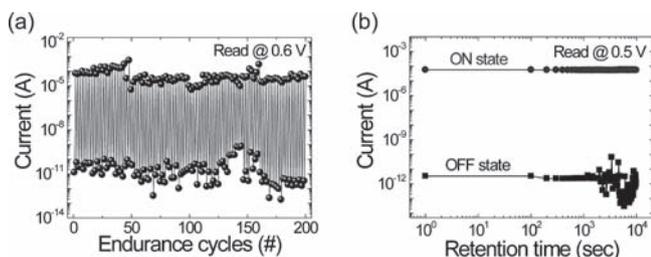
memory devices (see Experimental section for detailed information). The electrical characteristics of the 100 nm-scale memory device are shown in Figure 4b. The device was first programmed with a single sweep mode biased from 0 to 4 V, showing the current change from the OFF to the ON state. The ON state in the low voltage region (from 0 to 3 V) of the second single sweep (from 0 to 5 V) was stably maintained, and then the ON state was changed to the OFF state in the higher voltage region from 3 to 5 V. Sequential I–V curves (the third and fourth sweeps) also tracked the previous I–V curves. Notably, in comparison with 2 μm-scale memory devices, a reduction in the ON current level was observed in the 100 nm-scale memory devices, which was attributed to the decrease in the device junction area. Nevertheless, an ON/OFF ratio of over 10^3 was still sufficient to distinguish each state of the 2 μm-scale memory devices. Compared with the relatively high yield of 2 μm-scale memory devices, the yield of 100 nm-scale memory devices was poor. As scaling down the device to nanoscale, the device yield seemed to be strongly affected by the surface morphology of the substrate. If the height of bottom electrodes is quite tall compared to the organic film thickness, surface morphology after spincoating becomes wavy; this makes the metal transfer process more difficult. In particular, the problem became serious in 100 nm-scale memory devices due to the decreased contact area for holding the metals. To solve such a problem, incorporation of a planarization layer between the bottom electrodes to have a flat surface prior to the DMT process is scheduled.

In summary, we demonstrated the fabrication and use of unipolar organic resistive memory devices in an 8 × 8 array using a nonaqueous direct metal-transfer method to pattern the top electrodes. This method has the advantage of avoiding the solution processes required in conventional optical lithography, which could damage the underlying organic active layers. The fabricated organic memory devices with a 2 μm junction size exhibited a high ON/OFF ratio, stable switching characteristics, and good endurance and retention properties. Memory
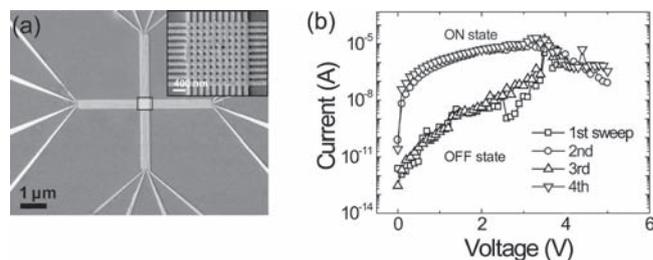

Figure 3. Memory performance data of 2 μm-scale organic memory devices. (a) Endurance cycle characteristics in repetitive DC sweep mode. (b) Retention characteristics.

Figure 4. (a) Scanning electron microscopy (SEM) image of 100 nm-scale organic memory devices in an 8 × 8 array structure. The inset SEM image shows an overview of the entire area of the memory cells. (b) I–V characteristics of 100 nm-scale organic memory device.

devices with a 100 nm junction size were also fabricated using the same method, demonstrating highly integrated organic memory device applications at the nanometer scale.

Experimental Section

Fabrication of stamp and bottom electrodes: The stamp was prepared on a transparent glass substrate for alignment with the bottom electrodes. The lines of the 2 µm stamp were fabricated by photolithography and subsequent reactive ion etching (RIE) processes. An Si/SiO$_2$ substrate was used for the formation of the bottom electrodes. Photoresist patterns with a 2 µm line width were formed by photolithography followed by the deposition of a 65 nm-thick Al layer using an electron-beam evaporator. The Al bottom electrode lines were elaborated using a standard lift-off process.

In the case of the devices with a 100 nm line width, a master silicon stamp was first generated by electron-beam lithography using a half-pitch of 100 nm and then duplicated as a transparent borosilicate stamp by nanoimprinting and subsequent RIE processes. Prior to imprinting, the stamp surface was coated with a releasing material, CF$_3$(CF$_2$)$_5$(CH$_2$)$_2$SiCl$_3$ (tridecafluoro-1,1,2,2-tetrahydroctyltrichlosilane), to aid master silicon stamp detachment from the imprinted resist.[28] UV-based nanoimprinting was employed at a pressure of 5 bar for 12 min on a formulated imprint resist to pattern the bottom electrodes and duplicate the transparent stamp.[29]

Preparation of organic active layers: To elaborate an organic active film, biphenyltetracarboxylic acid dianhydride p-phenylene diamine (BPDA-PPD), used as a polyimide (PI) precursor, was dissolved in N-methyl-2-pyrrolidone (NMP). A BPDA-PPD:NMP weight ratio of 1:4 was used for the fabrication of the 2 µm devices, whereas a weight ratio of 1:5 was used for the fabrication of the 100 nm organic memory devices. A solution of 1 wt% 6-phenyl-C61 butyric acid methyl ester (PCBM) was then prepared in NMP. The PI:PCBM composite solution for the 2 µm scale devices was made by mixing PI and the PCBM solution at a 4:1 weight ratio, whereas the solution was mixed at a 2:1 weight ratio for the 100 nm organic memory devices. To achieve reliable resistive switching effect in the 100 nm-scale devices, our memory devices needed an optimization for active material, which involves the blending ratio of BPDA-PPD and PCBM in NMP solvent. The prepared composite solution was spin-coated onto the bottom electrodes at 4000 rpm for 40 s after a UV-ozone treatment for 5 min, and then the substrate was soft baked at 50 °C for 1 min.

Fabrication of top electrodes: The top electrode lines were patterned using the direct metal-transfer method. The fabricated stamp was first coated with a monolayer of releasing material, as described above, to facilitate the easy transfer of the metal layer to the organic layer, and then a 40 nm-thick Au layer was deposited onto the stamp. The stamp coated with the Au film was vertically aligned over the substrate and the metal patterns were transferred from the stamp onto the substrate by applying a pressure of ~2.2 MPa at a temperature of 100 °C for 20 min under vacuum. Conformal contact between the organic film and the stamp surface is essential to achieve uniform metal transfer over the entire active area. Also, heat treatment should be accompanied during the metal transfer process, which makes the organic film sticky. The sticky organic film is favorable for the successful metal transfer. The stamp was then detached from the substrate and the completed devices were hard-baked at 300 °C for 30 min under a nitrogen atmosphere. All the electrical measurements were performed using a semiconductor characterization system (Keithley 4200-SCS) in a nitrogen glove box at room temperature.

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