Nanotechnology **20** (2009) 025201 (5pp) doi:10.1088/0957-4484/20/2/025201

Resistive switching characteristics of polymer non-volatile memory devices in a scalable via-hole structure

Tae-Wook Kim, Hyejung Choi, Seong-Hwan Oh, Minseok Jo, Gunuk Wang, Byungjin Cho, Dong-Yu Kim, Hyunsang Hwang and Takhee Lee[1]

Heeger Center for Advanced Materials, Department of Materials Science and Engineering, Gwangju Institute of Science and Technology, Gwangju 500-712, Korea

E-mail: tlee@gist.ac.kr

Received 5 August 2008, in final form 9 October 2008
Published 9 December 2008
Online at stacks.iop.org/Nano/20/025201

Abstract

The resistive switching characteristics of polyfluorene-derivative polymer material in a sub-micron scale via-hole device structure were investigated. The scalable via-hole sub-microstructure was fabricated using an e-beam lithographic technique. The polymer non-volatile memory devices varied in size from $40 \times 40\ \mu m^2$ to $200 \times 200\ nm^2$. From the scaling of junction size, the memory mechanism can be attributed to the space–charge-limited current with filamentary conduction. Sub-micron scale polymer memory devices showed excellent resistive switching behaviours such as a large ON/OFF ratio ($I_{ON}/I_{OFF} \sim 10^4$), excellent device-to-device switching uniformity, good sweep endurance, and good retention times (more than 10 000 s). The successful operation of sub-micron scale memory devices of our polyfluorene-derivative polymer shows promise to fabricate high-density polymer memory devices.

S Supplementary data are available from stacks.iop.org/Nano/20/025201

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Polymer materials have been developed as active components in a variety of device applications, such as organic light-emitting diodes, thin-film transistors, memory devices, photovoltaic cells, and sensors [1–5]. Among these applications, polymer non-volatile memory appears highly attractive, owing to its potential usage in data storage media [6–12]. In particular, polymer memory devices have attracted a lot of attention due to their simple structure, three-dimensional stacking capability, good scalability, high mechanical flexibility, and low fabrication cost.

Until now, most research on polymer memory devices has focused on the synthesis of conjugated polymer materials as memory elements [13–16] or the identification of appropriate ratios between polymer materials and metallic nanoparticles in a blend of the two [17–19]. Basic device structures for electrical characterizations were typically in the form of unit devices or cross-bar-type devices in which the active polymer memory elements were vertically sandwiched between two metallic electrodes [6–19]. The junction of the polymer memory devices has mainly been defined by the size of the shadow mask during the top electrode metallization; thus it has been hard to reduce the active cell size below the sub-micron scale. Junctions in sub-micron size have only been characterized by conducting atomic force microscopy (CAFM) [20, 21]. However, it is not trivial to evaluate the detailed memory performance of polymer materials with CAFM because the possible measurements are limited to current–voltage (I–V) sweeps or current images which are based on simple contacts or scanning of the conducting tip on the polymer layer.

The scaling issue has been one of the important research topics in many emerging memory technologies such as ferroelectric random access memory (FRAM), magneto-

[1] Author to whom any correspondence should be addressed.

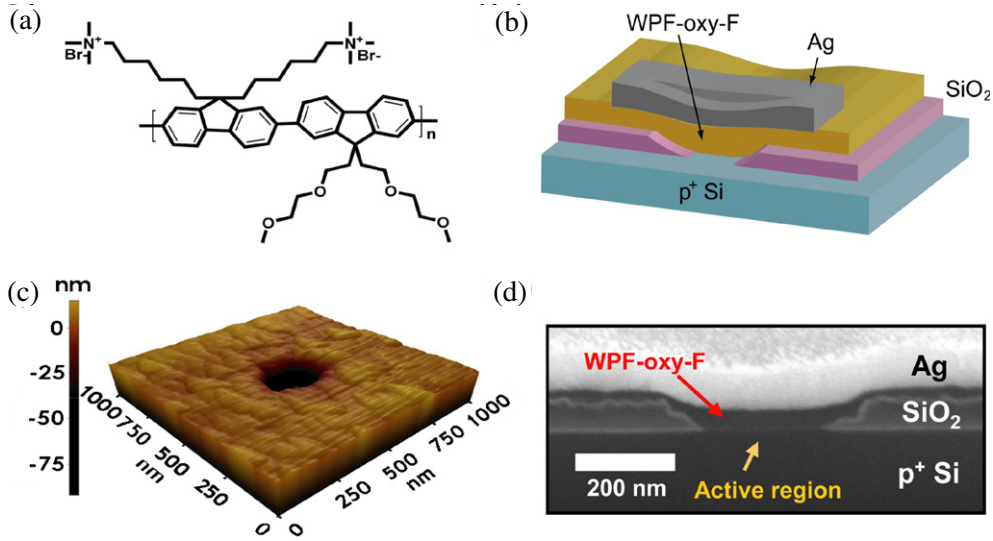

Figure 1. (a) Chemical structure of WPF-oxy-F polyfluorene derivative. (b) Schematic of a polymer memory device in a via-hole structure. (c) AFM image of a via-hole of area 200 × 200 nm^2. (d) SEM image of a tilt view of a via-hole polymer memory device.

resistive RAM (MRAM), phase-change memory (PRAM) and resistive change RAM (RRAM). Generally, these memories are based on inorganic materials which have robustness against organic solvent. Therefore, downscaling of such memory devices was successfully achieved by using the conventional CMOS process. On the other hand, polymer materials are easily dissolved by organic solvents; thus the conventional lithography method has not been appropriate to pattern polymer materials. Recently, Kwan *et al* reported a photo cross-linkable copolymer that can be directly patterned using the conventional photolithography process [22]. They successfully demonstrated the fabrication of 4 × 4 μm^2 memory cells to show the potential of high-density memory devices [22]. However, this fabrication process is appropriate only for a specific polymer material that is robust against specific organic solvents. In addition, it would be difficult to minimize the feature size to sub-micron scale using conventional photolithography techniques. Although various efforts have been made to fabricate polymer memory devices on the sub-micron size [20–22], the downscaling of polymer memory devices is still insufficient for high-density polymer memory applications.

To our knowledge, there have been few reports on the characterization of polymer materials in a sub-micron scale device structure or on whether the memory performance can be sustained when the device size is reduced to sub-micron scale. In particular, the characterization of memory properties of sub-micron scale devices will enhance understanding of the mechanisms of memory operation. In this point of view, scaling is one of the important issues for high-density polymer non-volatile memory device applications; thus it is essential to understand the scaling effects of polymer memory devices from micron scale to sub-micron scale.

In this study, we suggest a via-hole structure as a scalable test-bed for switching characterization of polymer materials. Polymer memory devices varying from micron scale to sub-micron scale were produced using an e-beam lithography technique. We present the high-performance resistive switching characteristics of polymer non-volatile memory devices in the sub-micron scale via-hole structure and demonstrate scalability towards potential applications in high-density polymer memory devices.

2. Experimental details

Polymer memory devices in a via-hole structure were fabricated on a heavily doped p-type (100) silicon (p$^+$ Si) substrate (0.001–0.015 Ω cm). After the typical ultrasonic cleaning process with acetone, methanol, and deionized (DI) water, the silicon substrate was treated via a diluted HF-last process to remove the native oxide layer. To make via-hole structures, ∼100 nm thick silicon oxide film was deposited on the silicon substrate using plasma-enhanced chemical vapour deposition (PECVD). Then, an e-beam lithography technique was used to define the active area of the polymer memory devices in the via-hole structures which have five different areas: 40 × 40 μm^2, 8.5 × 8.5 μm^2, 4.5 × 4.5 μm^2, 1 × 1 μm^2, 500 × 500 nm^2, and 200 × 200 nm^2. To expose the bottom electrode through a via-hole, the silicon oxide film was etched out using 6:1 buffered oxide etchant (BOE). Finally, to fill the via-hole with the polymer memory materials using a spin-coating method, we used the isotropic property of a wet etching process. As a result of wet etching, the wall of the via-hole is inclined, so that the polymer material can easily be spin coated and filled in the via-hole without any pores or defects (figures S3, see supplementary information (available at stacks.iop.org/Nano/20/025201)). As a polymer memory layer, poly[(9,9-bis((6′-(*N*,*N*,*N*-trimethylammonium)hexyl)-2,7-fluorene)-*alt*-(9,9-bis (2-(2-methoxyethoxy)ethyl)-fluorene)] dibromide (denoted as WPF-oxy-F), schematically shown in figure 1(a), was synthesized by a palladium-catalyzed Suzuki coupling reaction method [23]. WPF-oxy-F was first dissolved in methanol at a concentration of 5 mg ml^{-1} and

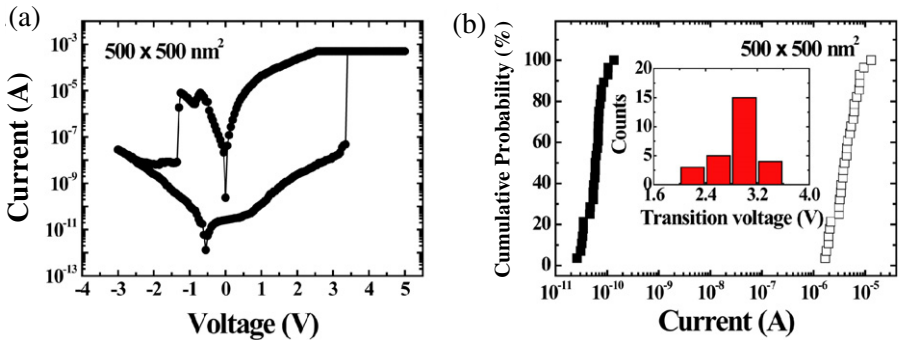

Figure 2. (a) Semilogscale I–V characteristics of a polymer memory device with a 500 × 500 nm^2 via-hole. (b) A cumulative probability data set for polymer memory devices with a 500 × 500 nm^2 via-hole (28 devices), showing a good device-to-device switching uniformity. The inset figure shows the histogram of the OFF-to-ON transition for polymer memory devices with a 500 × 500 nm^2 via-hole.

then was spin coated on the substrate. The typical spin-coating condition was 2000 rpm for 30 s. Post baking was performed at 150 °C for 20 min on a hotplate in a nitrogen-filled glove box. The typical thickness of the WPF-oxy-F film in the via-hole was found to be ∼70 nm. To make the top electrodes on the polymer layer in the via-hole structure, a shadow mask was aligned and a 100 nm thick Ag layer was deposited using a thermal evaporator under a pressure of 10^{-6} Torr. The current–voltage (I–V) measurements were carried out using a semiconductor parameter analyzer (Agilent Technology 4155C). The write–read–erase–read cycles were measured with a two-channel pulse generator (Agilent Technology 81104A) and a two-channel oscilloscope (Tektronix TDS 3054B).

3. Results and discussion

A schematic of the polymer memory device is shown in figure 1(b), illustrating the Ag/WPF-oxy-F/p$^+$ Si layer in the via-hole. The active area of the memory device can be easily defined by the area of bottom electrode (p$^+$ Si) that is exposed through the via-hole. Because all the area except the via-hole is protected by a SiO_2 layer, the via-hole is the only way for current to flow (figure S4(a), see supplementary information (available at stacks.iop.org/Nano/20/025201)). Figure 1(c) shows the AFM image of a via-hole device with an active area of 200 × 200 nm^2. Figure 1(d) is the scanning electron microscopy (SEM) image of a tilt view of a polymer memory device. Due to the inclined wall shape made by the wet etching process, the via-hole can be completely filled with WPF-oxy-F without any pinholes or bubbles (figure S3, see supplementary information (available at stacks.iop.org/Nano/20/025201)). It was also observed that the Ag (top electrode) did not penetrate into the WPF-oxy-F layer. The SEM image in figure 1(d) clearly shows that the three layers of Ag/WPF-oxy-F/p$^+$ Si in the via-hole are well separated (figure S3, see supplementary information (available at stacks.iop.org/Nano/20/025201)).

Figure 2(a) shows a representative I–V characteristic of a single-layer Ag/WPF-oxy-F/p$^+$ Si memory device in the via-hole of area 500 × 500 nm^2. Previous reports on the resistive switching of a WPF-oxy-F based planar-type device (without a via-hole structure; figure 4(S)(b), see supplementary information (available at stacks.iop.org/Nano/20/025201)) showed excellent electrical bistability with a high ON/OFF ratio (e.g., I_{ON}/I_{OFF} ∼ 10^4 at 0.3 V) [15, 16]. The basic operation of our memory device was well explained by the space–charge-limited current (SCLC) with filamentary conduction from the I–V characteristics and current images [16]. Although the device structure used in this work is different from that in previous work [16], similar resistive switching behaviour was observed within the voltage range −3–5 V. When a positive bias from 0 to 5 V is applied to the top electrode, the trap sites in the polymer layer begin being filled by electrons and more traps become occupied as the current flow increases. The trap-filling process creates high-current paths which in turn lead to electromigration and filamentary conduction paths [16]. On the other hand, a negative bias on the top electrode retracts filamentary conduction and leaves the trap sites empty, showing an abrupt decrease of current [16]. In addition, the distributions of current values for the ON state (low-resistance state) and OFF state (high-resistance state) in sub-micron scale via-hole devices were found to be very narrow. As shown in figure 2(b), the current values of all the 28 measured devices (500 × 500 nm^2) were distributed within an order of magnitude, which indicates excellent device-to-device switching uniformity. This excellent uniformity may be due to the decrease of defects at the sub-micron scale active area. The transition from OFF to ON in most of sub-micron scale polymer memory devices occurred in the range between 3.2 and 1.8 V (inset of figure 2(b)). Note that some reports have explained that the bistability of the organic non-volatile memory device is originated from an interface oxide layer such as Al_2O_3 [24–26]. In this work, in order to minimize or eliminate the effect of native oxide on the p$^+$ Si and Ag electrode, we carefully removed native oxide and spin coated the WPF-oxy-F in a glove box system filled with N_2. In addition, the Ag top electrode was deposited on the WPF-oxy-F film with as small a delay as possible.

The Ag/WPF-oxy-F/p$^+$ Si devices in the via-hole structure also showed an excellent scalability that makes them suitable for high-density polymer memory device applications. As shown in figure 3(a), the current value of the ON state

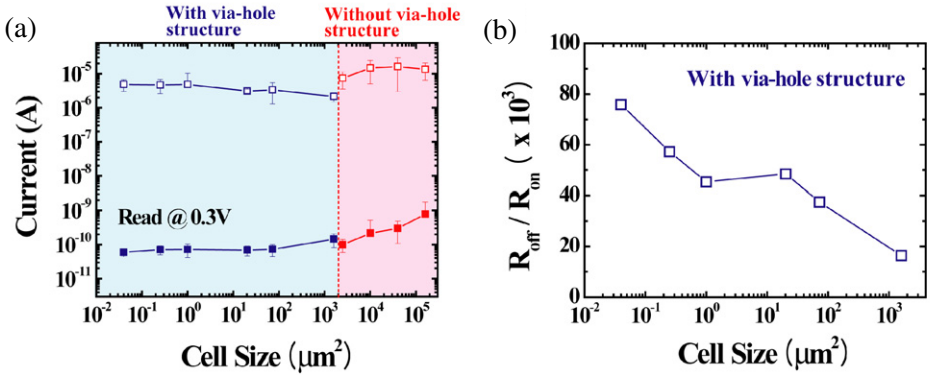

Figure 3. (a) Current values of the ON and OFF states of polymer memory devices as a function of active area. (b) Dependence of the OFF/ON resistance ratio of polymer memory devices as a function of active area.

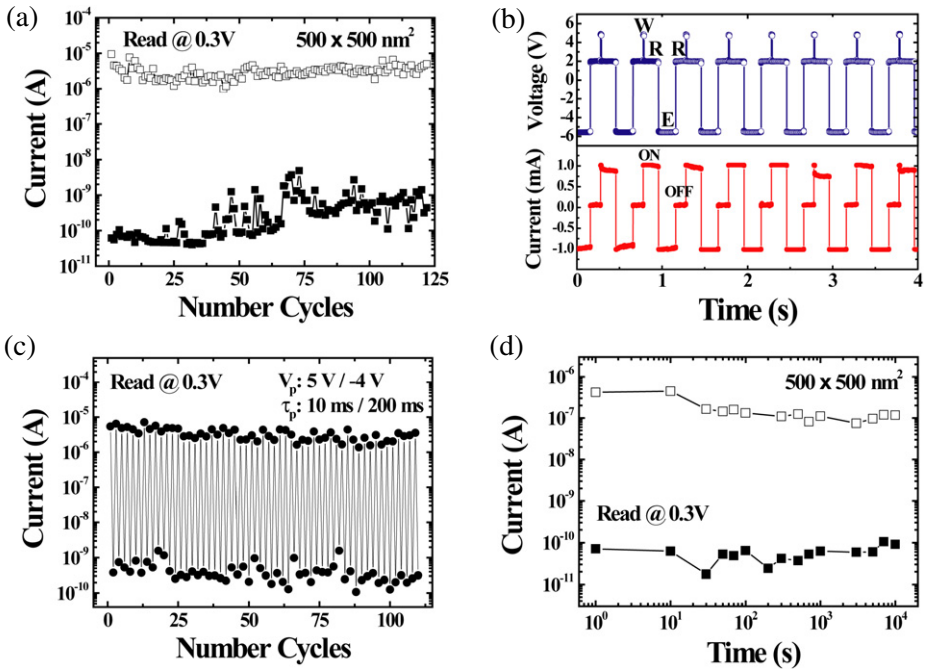

Figure 4. (a) Sweep endurance test results of a polymer memory device with a 500 × 500 nm^2 via-hole. (b) Write–read–erase–read (W–R–E–R) cycles for a polymer memory device with a 500 × 500 nm^2 via-hole. The top and bottom curves indicate the applied voltage and the corresponding current response, respectively. (c) Switching cycle of a polymer memory device with a 500 × 500 nm^2 via-hole by consecutive voltage pulses. ON and OFF states were alternated with a 5 V pulse (writing process) and a −4 V voltage pulse (erasing process) with pulse duration time of 10 ms and 200 ms, respectively. (d) Retention characteristics of the ON and OFF states measured at room temperature.

did not change with variation of the active area (about 5 μA), whereas the current value of the OFF state decreased slightly as the active area decreased. This is consistent with the results of our previous report on the polymer memory devices made as planar-type structure (without via-hole structure) with the active area ranging from 400 × 400 to 50 × 50 μm^2 [16]. In our previous work, we clearly observed that the current flow through the WPF-oxy-F film was localized from investigating CAFM images of the ON and OFF states [16]. Since the formation of localized current at the first spot (filament) may prevent the activation of current flows through other spots, the ON state current shows area independent behaviour. On the other hand, because the OFF state current flow is limited by the leakage current, it is proportional to the active area of the device. Therefore, the ON/OFF ratio ($R_{\mathrm{OFF}}/R_{\mathrm{ON}}$) also increased slightly as the active area decreased, as shown in figure 3(b). All these observations indicate that localized current paths (conducting filaments) are formed and affect the resistive switching behaviour even in sub-micron scale via-hole polymer memory devices. If the resistive switching behaviour is governed only by filamentary conduction, the OFF state current should scale with the active area [27, 28]. Indeed, the OFF state current in via-hole structures was observed to be slightly proportional to the active area in our polymer material (WPF-oxy-F). This dependence of both the OFF state current and the ON/OFF ratio ($R_{\mathrm{OFF}}/R_{\mathrm{ON}}$) on the active area implies

that SCLC with filamentary conduction is the origin of the resistive switching behaviour [16].

In order to investigate the performance of sub-micron scale polymer memory devices, a series of characterizations including sweep endurance, write–read–erase–read cycle tests, switching cycles with consecutive pulses, and retention tests were carried out. All tests were performed on the via-hole devices of area 500 × 500 nm^2. Figure 4(a) shows the sweep endurance results. More than 100 voltage sweeps were performed with the same sweep conditions (voltage range from −3 to 5 V). The ON and OFF current values were well separated with a high ON/OFF ratio ($\sim 10^4$) during more than 100 sweeps. In addition, the repeating cycle test consisting of write, read, erase, and read was performed, and the results are shown in figure 4(b). The test conditions were a 10 ms write pulse at 4 V, a 200 ms erase pulse at −6 V, and a read voltage at 2 V. According to the applied voltage sequence for write, read, and erase pulses, the device showed the corresponding current responses (bottom curve in figure 4(b)), indicating reliable switching behaviour. We also performed endurance measurements with consecutive single voltage pulses, as shown in figure 4(c). To examine the operation of the memory device, ON and OFF states were alternated with a 5 V pulse (writing process) and a −4 V voltage pulse (erasing process) with pulse duration time of 10 ms and 200 ms, respectively. In this case, the duration times of both the writing and erasing pulses were the minimum times for stable switching of the device showing the largest ON/OFF ratio. During more than 100 voltage pulse repetitions, the memory device showed well-separated current states on each voltage pulses, exhibiting an ON/OFF ratio of more than 10^3 read at 0.3 V. No significant degradation of each current state was observed. In addition, after the polymer memory device was written or erased, current values for both ON and OFF states were maintained for longer than 10^4 s without any significant degradation under ambient conditions at room temperature (figure 4(d)).

4. Conclusions

In summary, we investigated WPF-oxy-F non-volatile memory devices in a scalable via-hole structure. The devices, ranging from micron scale to sub-micron scale, exhibited excellent non-volatile memory performance such as a large ON/OFF ratio ($I_{ON}/I_{OFF} \sim 10^4$), and good sweep endurance, retention times (more than 10 000 s), and device-to-device switching uniformity. These electrical characteristics for sub-micron scale devices and the scalability suggest that WPF-oxy-F has potential for use in high-density sub-micron scale polymer memory devices. In addition, the scalable via-hole is a good test-bed structure to evaluate the electrical characteristics of polymer memory devices from micron scale to sub-micron scale.

Acknowledgments

This work was supported by the National Research Laboratory (NRL) Programs of the Korea Science and Engineering Foundation (KOSEF), the Program for Integrated Molecular System at GIST, and the SystemIC2010 project of Korea Ministry of Knowledge Economy.

References

[1] Müller C D, Falcou A, Reckefuss N, Rojahn M, Wiederhirn V, Rudati P, Frohne H, Nuyken O, Becker H and Meerholz K 2003 *Nature* **421** 829
[2] Chen Y, Jung G Y, Ohlberg D A A, Li X, Stewart D R, Jeppesen J O, Nielsen K A, Stoddart J F and Williams R S 2003 *Nanotechnology* **14** 462
[3] Kim J Y, Lee K, Coates N E, Moses D, Nguyen T Q, Dante M and Heeger A J 2007 *Science* **317** 222
[4] Darlinski G, Böttger U, Waser R, Klauk H, Halik M, Zschieschang U, Schmid G and Dehm C 2005 *J. Appl. Phys.* **97** 093708
[5] Lee T W, Byun Y, Koo B W, Kang I N, Lyu Y Y, Lee C H, Pu L and Lee S Y 2005 *Adv. Mater.* **17** 2180
[6] Bozano L D, Kean B W, Beinhoff M, Carter K R, Rice P M and Scott J C 2005 *Adv. Funct. Mater.* **15** 1933
[7] Karakawa M, Chikamatsu M, Yoshida Y, Azumi R, Yase K and Nakamoto C 2007 *Macromol. Rapid Commun.* **28** 1479
[8] Tu C H, Lai Y S and Kwong D L 2006 *IEEE Electron Device Lett.* **27** 354
[9] Bandhopadhyay A and Pal A J 2003 *J. Phys. Chem.* B **107** 2531
[10] Ouyang J, Chu C W, Szmanda C R, Ma L and Yang Y 2004 *Nat. Mater.* **3** 918
[11] Tseng R J, Tsai C, Ma L, Ouyang J, Ozkan C S and Yang Y 2006 *Nat. Nanotechnol.* **1** 72
[12] Weitz R T, Walter A, Engl R, Sezi R and Dehm C 2006 *Nano Lett.* **6** 2810
[13] Pearson C, Ahn J H, Mabrook M F, Zeze D A, Petty M C, Kamtekar K T, Wang C, Bryce M R, Dimitrakis P and Tsoukalas D 2007 *Appl. Phys. Lett.* **91** 123506
[14] Ling Q D, Kang E T, Neoh K G, Chen Y, Zhuang X D, Zhu C and Chan D S H 2008 *Appl. Phys. Lett.* **92** 143302
[15] Kim T W, Oh S H, Choi H, Wang G, Hwang H, Kim D Y and Lee T 2008 *IEEE Electron Device Lett.* **29** 852
[16] Kim T W, Oh S H, Choi H, Wang G, Hwang H, Kim D Y and Lee T 2008 *Appl. Phys. Lett.* **92** 253308
[17] Son D I, Kim J H, Park D H, Choi W K, Li F, Ham J H and Kim T W 2008 *Nanotechnology* **19** 055204
[18] Tseng R J, Baker C O, Shedd B, Huang J, Kaner R B, Ouyang J and Yang Y 2007 *Appl. Phys. Lett.* **90** 053101
[19] Yang Y, Ma L and Wu J 2004 *MRS Bull.* **29** 833
[20] Paul S, Kanwal A and Chhowalla M 2006 *Nanotechnology* **17** 145
[21] Kim J, Cho S, Choi S, Baek S, Lee D, Kim O, Park S M and Ree M 2007 *Langmuir* **23** 9024
[22] Kwan W L, Tseng R J, Wu W, Pei Q and Yang Y 2007 *IEDM Technical Digest* p 237
[23] Oh S H, Na S I, Nah Y C, Vak D, Kim S S and Kim D Y 2007 *Org. Electron.* **8** 773
[24] Verbakel F, Meskers S C J, Janssen R A J, Gomes H L, Cölle M, Büchel M and de Leeuw D M 2007 *Appl. Phys. Lett.* **91** 192103
[25] Billen J, Steudel S, Müller R, Genoe J and Heremans P 2007 *Appl. Phys. Lett.* **91** 263507
[26] Yook K S, Lee J Y, Kim S H and Jang J 2008 *Appl. Phys. Lett.* **92** 223305
[27] Lecomber P G, Owen A E, Spear W E, Hajto J, Snell A J, Choi W K, Rose M J and Reynolds S 1985 *J. Non-Cryst. Solids* **77/78** 1373
[28] Jo S H and Lu W 2008 *Nano Lett.* **8** 392