Logic inverters composed of controlled depletion-mode and enhancement-mode ZnO nanowire transistors

Gunho Jo, Woong-Ki Hong, Jongsun Maeng, Minhyeok Choe, Woojin Park, and Takhee Lee[a)]

Department of Nanobio Materials and Electronics and Department of Materials Science and Engineering, Gwangju Institute of Science and Technology, Gwangju 500-712, Republic of Korea

(Received 12 November 2008; accepted 10 April 2009; published online 1 May 2009)

We demonstrate ZnO nanowire logic inverters consisting of *n*-channel depletion-mode (D-mode) transistors and *n*-channel enhancement-mode (E-mode) transistors that are selectively controlled by smooth- and corrugated-surface ZnO nanowires grown on two different types of substrates via a vapor transport method. Our inverter circuits, by combination of both D-mode and E-mode ZnO nanowire devices, show desired voltage transfer characteristics with a high gain and robust noise margin in a simple circuit design with less power dissipation, which makes them superior to logic inverters based on single-mode nanowire transistors. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3127514]

One-dimensional semiconductor nanostructures are promising building blocks for nanoelectronic device applications, such as field effect transistors (FETs),[1,2] diodes,[3] sensors,[4] and logic circuits.[3,5–8] In particular, because FET is the basic component of logic circuits, nanowire FET-based logic devices have been recently demonstrated.[3,6,7] However, all of these logic circuits are based on nanowire FETs operating in the *n*-channel depletion-mode (D-mode) that exhibits nonzero current at zero gate bias and negative threshold voltages. In contrast, the *n*-channel enhancement-mode (E-mode) FETs, which have an off-current status at zero gate bias and positive threshold voltages, often have more advantages than the D-mode FETs because the E-mode FETs do not have a conducting channel at zero gate bias, leading to reduced power dissipation.[9–12] Furthermore, for wide application of nanowire FET-based logic circuits with a simple circuit design and high logic performance, both D-mode and E-mode FETs are often required.[9–12] To date, however, there have been no reports on logic circuits constructed from a combination of both D-mode and E-mode nanowire FETs because E-mode operation for nanowire-based FETs is usually rather difficult to achieve. Recently, we reported that D-mode and E-mode ZnO nanowire FETs can be adjusted by controlling the surface morphology of nanowires and trap states at the interface between the ZnO nanowires and the dielectric layer.[11,13]

In this letter, we demonstrate the use of ZnO nanowire logic inverters as a key element of logic circuits, which are composed of *n*-channel D-mode ZnO nanowire FETs as the load device and *n*-channel E-mode ZnO nanowire FETs as the driver device. The D-mode and E-mode ZnO nanowire transistors are selectively managed by smooth and corrugated ZnO nanowires grown on two different substrates, respectively. Our inverter scheme, consisting of both D-mode and E-mode nanowire FETs, allows for a simple circuit design with a high gain and robust noise margin for potential application of nanowire FET-based logic circuits.

ZnO nanowires were synthesized via a vapor transport method on two different types of substrates, an Au-coated *c*-plane sapphire (denoted as Au-sapphire) and an Au-coated gallium-doped ZnO film (denoted as Au-GZO film). Synthesis of ZnO nanowires by the vapor transport method has been reported in detail elsewhere.[13] The grown ZnO nanowires were characterized using scanning electron microscopy (SEM) and transmission electron microscopy (TEM). The upper insets of Figs. 1(a) and 1(b) show low magnification TEM images, which allow for comparison of the overall surface morphology of ZnO nanowires grown on two different types of substrates. The morphology of ZnO nanowires grown on Au-GZO film [Fig. 1(b)] are seen to be significantly rougher across the surfaces as compared to the ZnO nanowires grown on an Au-sapphire substrate [Fig. 1(a)]. High resolution TEM (HRTEM) was also used to characterize these two types of ZnO nanowires in greater detail. As shown in Figs. 1(a) and 1(b), lattice-resolved images and computed fast Fourier transform patterns (lower insets) obtained from the lattice fringes of ZnO nanowires indicate that both types of ZnO nanowires are single crystalline with a preferred growth direction of [0001].

In order to fabricate ZnO nanowire FETs and logic inverters composed from them [Fig. 1(c)], two types of ZnO

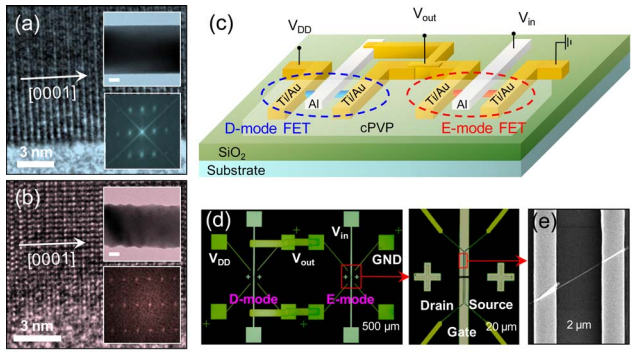

FIG. 1. (Color online) HRTEM images of (a) a smooth ZnO nanowire grown on Au-sapphire and (b) a corrugated ZnO nanowire grown on Au-GZO film. Insets show low magnification TEM images (upper) and computed fast Fourier transform patterns (lower). The scale bars are 20 nm in the upper insets. (c) Schematic illustration of logic inverter composed of D-mode and E-mode nanowire FETs. (d) Optical images of the fabricated inverters. (e) SEM image of a ZnO nanowire FET.

a)Electronic mail: tlee@gist.ac.kr.

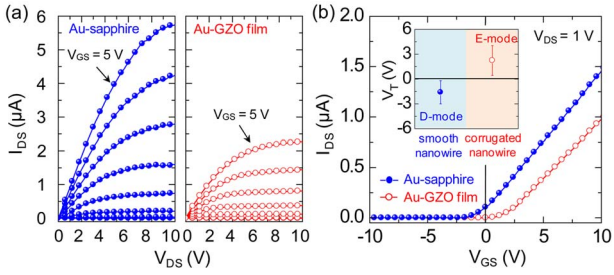

FIG. 2. (Color online) (a) I_{DS}-V_{DS} for *n*-channel D-mode FET made of ZnO nanowire grown on Au-sapphire (left side) and *n*-channel E-mode FET made of ZnO nanowire grown on Au-GZO substrate (right side), obtained at various values of V_{GS} from −1 to 5 V with 1 V step. (b) I_{DS}-V_{GS} curves measured at V_{DS}=1 V for D-mode ZnO nanowire FET (filled blue symbols) and E-mode ZnO nanowire FET (open red symbols). The inset shows statistical distribution of threshold voltages (V_T) of 23 smooth ZnO nanowires FETs and 19 corrugated ZnO nanowires FETs.

nanowires (i.e., smooth and corrugated nanowires) were selectively transferred to specific locations of the substrate defined by photoresist. Then, Ti (30 nm)/Au (40 nm) source and drain electrodes were fabricated using photolithography and the source and drain contact pads were protected by Kapton tapes during the formation of the gate dielectric layer. Cross-linked poly-4-vinylphenol (cPVP) was spin coated as a gate dielectric, followed by the deposition of an Al (50 nm) top gate electrode. A detailed description of the recipe for cPVP has been published elsewhere.[14] Finally, interconnected lines for logic inverters were patterned with a shadow mask or made by wire bonding. The current-voltage transfer characteristics of transistors and logic inverters were measured using a semiconductor parameter analyzer (Agilent B1500A) in an ambient atmosphere.

Figure 1(c) shows the schematic structure of a logic inverter that uses a D-mode ZnO nanowire FET for the driver and an E-mode ZnO nanowire FET for the load. Here, the smooth ZnO nanowires operate as D-mode transistors, whereas corrugated ZnO nanowires operate as E-mode transistors, which are explained in detail later. In the inverter shown in Fig. 1(c), one end of the D-mode transistor is connected to the power supply (V_{DD}) and one end of the E-mode transistor is grounded. The other ends of the D-mode and E-mode nanowire FETs are connected as output voltage (V_{out}), and the gate voltage of E-mode is used as the input (V_{in}). The polymer dielectric layer (cPVP) was used as a gate insulator for both types of nanowire FETs. It has been reported that the transistor characteristics of ZnO nanowire FETs with the cPVP polymer gate dielectric are comparable to ZnO nanowire FETs with the SiO_2 gate dielectric.[13,14] Figs. 1(d) shows the optical image of the actual inverters composed of D-mode and E-mode ZnO nanowire FETs, and Fig. 1(e) shows the SEM image of a ZnO nanowire FET (before cPVP coating) as a component of logic inverters.

Figures 2(a) and 2(b) show the output characteristics (I_{DS}-V_{DS}, source-drain current versus drain voltage) and the transfer characteristics (I_{DS}-V_{GS}, source-drain current versus gate voltage) of FETs made from smooth ZnO nanowires grown on the Au-sapphire substrate [left plot of Fig. 2(a)] and corrugated ZnO nanowires grown on the Au-GZO substrate [right plot of Fig. 2(a)]. As shown in Fig. 2(a), the I_{DS}-V_{DS} characteristics of both types of ZnO nanowire FETs exhibit well-defined linear regimes at low bias, and saturation regimes at high bias with typical electrical behavior of *n*-type FETs. Here, an interesting result is that electrical conductance and threshold voltage can be controlled by the surface morphology of the ZnO nanowires. The FET devices made from smooth ZnO nanowires grown on the Au-coated sapphire substrate operated as the normally on type, *n*-channel D-mode [blue symbols in Fig. 2(b)], which exhibit nonzero current at zero gate bias and a negative threshold voltage, indicating that a more negative gate bias should be applied to deplete carriers in the conducting channel. On the other hand, the FET devices made from corrugated ZnO nanowires grown on the Au-GZO film operated as the normally off type, *n*-channel E-mode [red symbols in Fig. 2(b)], which shows off-current status at zero gate bias and a positive threshold voltage, indicating that more a positive gate bias is needed to create the conducting channel. As compared to the smooth ZnO nanowires, the corrugated ZnO nanowires can generate a more significant fraction of the electron depletion region due to deep traps in the channel or at the interface between the ZnO nanowires and dielectric layer.[11,13] As a result, corrugated ZnO nanowire FETs exhibit positive threshold voltage (E-mode behavior). The threshold voltages of the particular D-mode and E-mode ZnO nanowire FETs demonstrated in Fig. 2(b) were found to be −0.5 and 1.8 V, respectively. The inset of Fig. 2(b) shows the statistical distribution of the threshold voltage position (i.e., D-mode or E-mode) of 23 FET devices made of smooth ZnO nanowires and 19 FET devices made of corrugated ZnO nanowires characterized in this study. Therefore, it can be said that, statistically, D-mode and E-mode ZnO nanowire FETs were well controlled by the nanowire surface-morphology, suggesting that controlled growth of nanowire surface can be a good method for selective adjustment of operational modes of ZnO nanowire-based transistors.

From transfer characteristics [Fig. 2(b)], the transconductance ($g_m = dI_{DS}/dV_{GS}$) and field effect mobility[15] [$\mu_e = L^2/C_{NW}V_{DS}\cdot(\partial I_{DS}/\partial V_{GS})$] were estimated to be 147 nS and 65 $cm^2/V\,s$ for the smooth nanowire FET and 140 nS and 67 $cm^2/V\,s$ for the corrugated nanowire FET, respectively. Here, L is the channel length of the nanowire and $C_{NW} = 2\pi\varepsilon_r\varepsilon_0 L/\cosh^{-1}[(r+h)/r]$ is the approximate gate-nanowire capacitance, r is the nanowire radius (~110 nm for the smooth nanowire and ~88 nm for the corrugated nanowire), h is the polymer dielectric layer thickness (200 nm), ε_0 is the permittivity of free space, and ε_r is the dielectric constant of cPVP (3.6).[14]

As mentioned previously, a combination of both E-mode and D-mode nanowire FETs is more preferable in logic circuits than circuits using a single-mode type of nanowire FETs.[10–12] Moreover, the following parameters of inverter circuits are important in order to satisfy performance criteria: (i) the V_{DD}, (ii) the threshold voltages of the load and the driver FETs, (iii) the device dimensions (e.g., channel length), and (iv) material parameters such as mobility and dielectric constant.[10,16] In our study, we particularly focused on selectively matching the threshold voltages for D-mode and E-mode nanowire FETs as the load and driver, respectively.

Figure 3(a) shows the typical voltage transfer characteristic (VTC) of a logic inverter made from two types of surface-controlled ZnO nanowire FETs operating under a supply voltage (V_{DD}) of 5 V. In the circuit diagram of the inverter circuit [inset of Fig. 3(a)], the *n*-channel D-mode

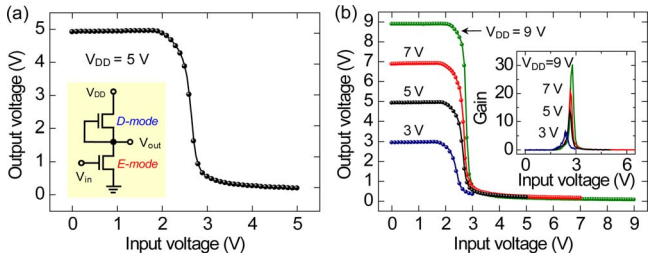

FIG. 3. (Color online) (a) VTC curve of a logic inverter composed of *n*-channel D-mode and *n*-channel E-mode ZnO nanowire FETs, obtained at V_{DD}=5 V. The inset shows an inverter circuit diagram. (b) VTC curves of the inverter obtained under various values of V_{DD} from 3 to 9 V with a 2 V step. The inset shows voltage gain curves derived from the various VTC curves.

smooth nanowire FET is a load device and the *n*-channel E-mode corrugated nanowire FET is a driver device. The inverter response to stage switching was clearly observed in the input voltage (V_{in}) range from low (0 V) to high (5 V), displaying its transition voltage (V_T) of ~2.6 *V*. At this V_T, $V_{in}=V_{out}$ on the VTC. When V_{in} is logical 0 ($V_{in}=0$ V), the driver (E-mode corrugated nanowire FET) is cut off and output voltage (V_{out}) is close to V_{DD} (logical 1). When V_{in} is logical 1 ($V_{in}=5$ V), the driver transistor is on with much less resistance than that of the load transistor (D-mode smooth nanowire FET), and the V_{out} is close to 0 V (logical 0). Furthermore, the gain ($-dV_{out}/dV_{in}$) of our inverter circuit is ~14, with well-matched noise margins (NMs) of 1.9 V (NM_L denotes noise margin low) and 2.0 V (NM_H denotes noise margin high). Note that gain is defined as the maximum slope of the transition between the high and low states, which is a measure of the capability of a inverter circuit,[10] and the noise margin is defined as the difference between the input and output in the high or low states at unity gain.[10,17] As compared with logic inverters based on single-mode transistors, our inverter circuit shows a nearly symmetric and identical VTC shape, which was made possible by matching the threshold voltages of both FETs working discretely at D-mode and E-mode.[10,17] Furthermore, the inverter consisting of D-mode only is usually more complex in circuit design because of the required additional element for the level shifter, thus consuming more power.[6,18] Additionally, the inverter consisting of all E-mode transistors has the low inverting gain and limited swing.[10] Therefore, our ZnO nanowire inverter scheme, composed of both D-mode and E-mode FETs allowing high gain and robust noise margin in a simple circuit configuration and low power dissipation, is more advantageous for a wide range of application in nanowire-based logic circuits.

Figure 3(b) shows VTCs of the inverter for various supply voltages (V_{DD}) from 3 to 9 V with a step of 2 V. The inverter gains appear to increase with an increase in supply voltage, ranging from 6.4 to 30.3 [the inset of Fig. 3(b)]. Higher gain means that the high to low logic transition is much sharper, from which one can expect a more acceptable logic operation for high speed circuit application.[7,19] Furthermore, as V_{DD} is increased, the resistance of the driver (E-mode FET) becomes smaller than that of the load device (D-mode FET). Thus, when V_{in} is logic 1 with a higher V_{DD}, the output voltage approaches that of the GND since more voltage drops across the load device. As a result, the inverter exhibits almost a full swing characteristic with increasing V_{DD}.

In summary, we demonstrate the ZnO nanowire logic inverter, which is composed of surface-morphology-controlled *n*-channel D-mode and E-mode ZnO nanowire FETs with a polymer dielectric layer. The inverter exhibits symmetric voltage transfer characteristics with a transition voltage of ~2.6 V (with a supply voltage of 5 V) at the switching region from 0 to 5 V, a gain of 14, and a good noise margin. Our inverter scheme composed of both D-mode and E-mode FETs, allowing a simple circuit configuration and less power dissipation, is more advantageous for nanowire-based logic circuits than circuits based on the single-mode nanowire FETs.

This work was supported by the Basic Research Promotion Fund of the Korea Research Foundation Grant, the Proton Accelerator User Program of Korea, and the National Research Laboratory (NRL) Program, and the National Core Research Center grant by the Korea Science and Engineering Foundation (KOSEF).

[1] S. Ju, A. Facchetti, Y. Xuan, J. Liu, F. Ishikawa, P. Ye, C. Zhou, T. J. Marks, and D. B. Janes, Nat. Nanotechnol. **2**, 378 (2007).
[2] A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. Mcintyre, P. Mceuen, M. Lundstrom, and H. Dai, Nature Mater. **1**, 241 (2002).
[3] W. I. Park, J. S. Kim, G.-C. Yi, and H.-J. Lee, Adv. Mater. (Weinheim, Ger.) **17**, 1393 (2005).
[4] E. Stern, J. F. Klemic, D. A. Routenberg, P. N. Wyrembak, D. B. Turner-Evans, A. D. Hamilton, D. A. LaVan, T. M. Fahmy, and M. A. Reed, Nature (London) **445**, 519 (2007).
[5] Y. Cui and C. M. Lieber, Science **291**, 851 (2001).
[6] R. M. Ma, L. Dai, H.-B. Huo, W.-J. Xu, and G. G. Qin, Nano Lett. **7**, 3300 (2007).
[7] D. Yeom, K. Keem, J. Kang, D.-Y. Jeong, C. Yoon, D. Kim, and S. Kim, Nanotechnology **19**, 265202 (2008).
[8] D. Wang, B. A. Sheriff, and J. R. Heath, Small **2**, 1153 (2006).
[9] R. M. Ma, L. Dai, and G. G. Qin, Appl. Phys. Lett. **90**, 093109 (2007).
[10] S.-M. Kang and Y. Lebliebici, *CMOS Digital Integrated Circuits*, 3rd ed. (McGraw-Hill, New York, 2003), p. 186–193.
[11] W.-K. Hong, D.-K. Hwang, I.-K. Park, G. Jo, S. Song, S.-J. Park, T. Lee, B.-J. Kim, and E. A. Stach, Appl. Phys. Lett. **90**, 243103 (2007).
[12] R. Wang, Y. Cai, C.-W. Tang, K. M. Lau, and K. J. Chen, IEEE Electron Device Lett. **27**, 793 (2006).
[13] W.-K. Hong, J. I. Sohn, D.-K. Hwang, S.-S. Kwon, G. Jo, S. Song, S.-M. Kim, H.-J. Ko, S.-J. Park, M. E. Welland, and T. Lee, Nano Lett. **8**, 950 (2008).
[14] S.-S. Kwon, W.-K. Hong, G. Jo, J. Maeng, T.-W. Kim, S. Song, and T. Lee, Adv. Mater. (Weinheim, Ger.) **20**, 4557 (2008).
[15] G. Jo, J. Maeng, T.-W. Kim, W.-K. Hong, M. Jo, H. Hwang, and T. Lee, Appl. Phys. Lett. **90**, 173106 (2007).
[16] B. K. Crone, A. Dodabalapur, R. Sarpeshkar, R. W. Filas, Y.-Y. Lin, Z. Bao, J. H. O'Neill, W. Li, and H. E. Katz, J. Appl. Phys. **89**, 5125 (2001).
[17] B. A. Sheriff, D. Wang, J. R. Heath, and J. N. Kurtin, ACS Nano **2**, 1789 (2008).
[18] G. H. Gelinck, H. E. A. Huitema, E. V. Veenendaal, E. Cantatore, L. Schrijnemakers, J. B. P. H. V. D. Putten, T. C. T. Geuns, M. Beenhakkers, J. B. Giesbers, B.-H. Huisman, E. J. Meijer, E. M. Benito, F. J. Touwslager, A. W. Marsman, B. J. E. V. Rens, and D. M. D. Leeuw, Nature Mater. **3**, 106 (2004).
[19] D. Wang, B. A. Sheriff, M. McAlpine, and J. R. Heath, Nano Res. **1**, 9 (2008).