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Noise in ZnO Nanowire Field Effect Transistors

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The noise power spectra in ZnO nanowire field effect transistors (FETs) were experimentally investigated and showed a classical $1/f$ dependence. A Hooge's constant of 5×10^{-3} was estimated. This value is within the range reported for CMOS FETs with high-k dielectrics, supporting the concept that nanowires can be utilized for future beyond-CMOS electronic applications from the point of view of device noise properties. ZnO FETs measured in a dry O_2 environment displayed elevated noise levels compared to in vacuum. At low temperature, random telegraph signals are observed in the drain current.

Keywords: Zinc Oxide, Nanowire, $1/f$ Noise, Random Telegraph Signal.

1. INTRODUCTION

Semiconductor nanowires (NWs) represent an important class of nanoscale building blocks for future beyond-CMOS electronics.[1] Scaling electronic devices to nano-scale dimensions may introduce unforeseen physical mechanisms that may seriously compromise device reliability. One fundamental factor that determines the performance and reliability of electronic devices is the signal-to-noise ratio, which poses the lower limit for device operation. Hence, a thorough understanding of the noise properties is critical for the successful design and integration of semiconducting nanowire functional units in nanoelectronics. Low frequency (f) noise, which contains important information about current transport and fluctuations in materials and devices, traditionally has been utilized as a quality and reliability indicator for semiconductor devices.[2–6] Recently, extensive low frequency noise characterizations of carbon nanotube field effect devices have been carried out, which has significantly improved our knowledge of the noise properties in these devices. However, so far there are only limited reports of noise characterizations of semiconductor nanowire devices despite the fact that such structures hold great promise for future nanoelectronic applications. In this study, we fabricate ZnO nanowire field effect transistors (FETs) and characterize their low frequency noise properties.

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2. EXPERIMENTAL DETAILS

ZnO nanowires were synthesized by thermally vaporizing a 1:1 ratio of ZnO powder (99.995%) and graphite powder (99%). The nanowires were removed from the substrate into solution by a brief sonication in ethanol and are then dropped onto a 100 nm thick, thermally grown, oxide on a highly doped p-type silicon substrate that can be used as a gate electrode. Ti/Au (30 nm/200 nm) contacts were deposited by using an electron beam evaporator and defined by standard photolithography and a lift-off process to form the source and drain electrodes. The distance between source and drain electrodes is approximately 4 μm. Current–voltage characteristics of the ZnO NW FETs were measured by using a semiconductor parameter analyzer. The low frequency noise characterization for these devices was performed by using a typical noise measurement setup composed of a low noise DC biasing source, a low noise current amplifier, and a dynamic spectrum analyzer. All of the $1/f$ noise measurements were carried out at room temperature and under moderate vacuum (~4 mTorr) unless otherwise mentioned. The random telegraph signal is measured at 4 K and in high vacuum by using a high speed oscilloscope.

3. RESULTS AND DISCUSSION

Figure 1(a) shows typical drain current versus drain voltage (I_{ds}–V_{ds}) characteristics of a ZnO NW FET device at different gate biases V_{gs}, where V_{gs} was applied to the

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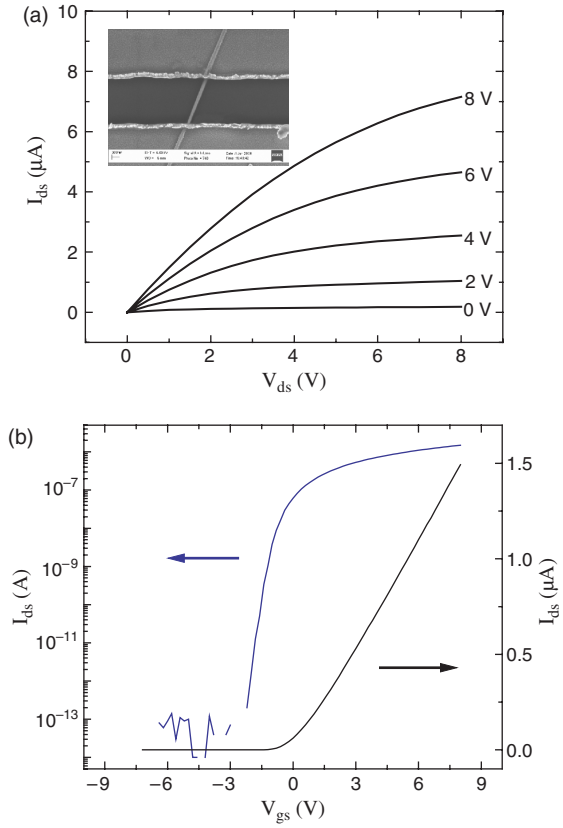

Fig. 1. (a) Typical I_d–V_d characteristics of a ZnO NW FET at gate biases of 0 V, 2 V, 4 V, 6 V, and 8 V measured at room temperature and under a vacuum of 4 mTorr. The inset shows the SEM image of a typical ZnO NW FET device. (b) Semi-logarithmic (left axis) and linear (right axis) plots of the I_d–V_g characteristic of the same device at a drain bias of 1 V.

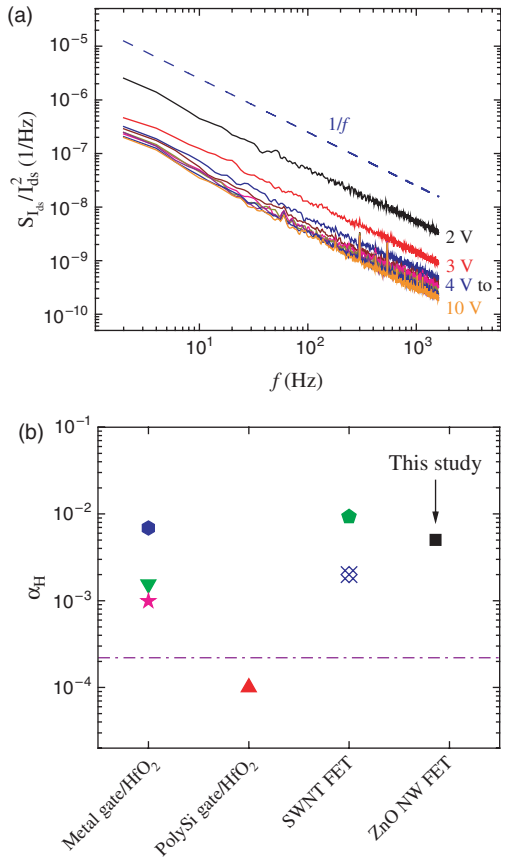

Fig. 2. (a) Typical normalized drain current noise power spectra at gate biases from 2 V to 10 V measured in the vacuum. $V_d = 1$ V and the frequency range is from 1 Hz to 1.6 kHz. The dashed line indicates the ideal $1/f$ dependence. (b) Summary plot of the Hooge's constant obtained in this study (black square) with previously published data for poly-silicon gate/HfO_2,[8] metal gate/HfO_2,[9] and single-wall nanotube FET devices.[7, 10] Different values of the same type of device are from different reports. The dash-dotted line shows the ITRS requirement on α_H for the 45 nm technology node.

silicon substrate in a back gate configuration. The conduction channel in this particular FET device is a ZnO NW of diameter of ∼140 nm with a nominal channel length (L) of 4 μm. Figure 1(b) shows the drain current versus gate voltage (I_{ds}–V_{gs}) characteristics of the same device at a fixed drain bias of 1 V. These characteristics display the expected n-type semiconducting transport behavior. From the I_{ds}–V_{gs} characteristics, a gate threshold voltage (V_{th}) of 0.05 V was extracted. The on/off ratio of this device at $V_{ds} = 1$ V is ∼10^7 (comparing I_{ds} at $V_{gs} = 8$ V and −3 V) and the subthreshold slope is ∼270 mV/decade.

Low frequency noise measurements of the ZnO NW FETs were carried out to study the current fluctuations in single nanowire devices. Figure 2(a) shows typical normalized drain current noise power spectra ($S_{I_{ds}}/I_{ds}^2$) at selected gate biases measured in vacuum. The drain bias was kept at 1 V and the frequency range was varied from 1 Hz to 1.6 kHz. For $1/f$ type fluctuations, the noise behavior can be described by[3]

$$S_{I_{ds}} = \frac{AI_{ds}^2}{f^\beta} \quad (1)$$

where A is the noise amplitude and the frequency exponent β is ideally 1. As shown in Figure 2(a), ZnO NW FET exhibited $1/f$ noise behavior with β values in the range of 0.92 to 1.02, which were obtained by doing linear fits to each spectrum in Figure 2(a). As a comparison, a dashed line indicating ideal $1/f$ dependence is also plotted in this figure. No Generation-Recombination (GR) noise was observed for our devices at room temperature as long as $V_g \geq V_{th} + 1$ V. From the data in Figure 2(a) the noise amplitude A can be obtained at $f = 1$ Hz according to Eq. (1). The noise amplitude decreases almost linearly at low gate biases and becomes saturated at high gate biases. In summary, noise characterizations of ZnO NW FETs at different gate voltages reveal that the noise behavior in the devices at low frequencies is $1/f$ type, and the corresponding noise amplitudes are dependent on the gate modified carrier numbers in the devices.

According to Hooge's empirical law, the $1/f$ noise amplitude can be expressed as[2]

$$A = \frac{\alpha_H}{N} \quad (2)$$

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where α_H is the Hooge's constant and N is the total carrier number in the system. This relationship was introduced to describe the $1/f$ noise in homogenous bulk materials, and α_H can be used to compare $1/f$ noise in different systems regardless of the specific device parameters and measurement conditions. For bulk materials α_H is typically on the order of 10^{-3}. By using Eq. (1) and the expression of the gate capacitance, following the model of the gate capacitance outlined in Ref. [7], the inverse of A can be expressed as

$$\frac{1}{A} = \frac{C_g L}{e\alpha_H}|V_g - V_{th}| \quad (3)$$

α_H is determined to be $\sim 5 \times 10^{-3}$ for the ZnO NW FET device. Figure 2(b) shows the Hooge's constant of the ZnO NW FETs, compared with previously published data of poly-silicon gate/HfO_2,[8] metal gate/HfO_2,[9] and single-wall nanotube FET devices.[7, 10] The dash-dotted line shows the ITRS requirement on α_H for the 45 nm technology node. As can be seen from Figure 2(b), the Hooge's constant of our device is similar to values reported recently for carbon nanotube FETs. Despite the nanowires' much higher surface-to-volume ratio, the obtained α_H is also comparable to that of future type CMOS FETs with high-k materials, such as HfO_2, as gate dielectrics. This comparison of NW FET noise data with that measured in other emerging device technologies supports the concept that, from the point of view of device noise properties, NWs can be used as device components for beyond CMOS electronic applications.

Several groups have previously reported the oxygen sensing properties of ZnO NWs. In order to investigate the change of the noise characteristics of ZnO NW FETs under the oxygen environment, we have performed noise measurements in a dry oxygen environment. The devices that were originally tested in vacuum were left in dry oxygen under a pressure of 900 Torr for 2 days before the measurements to ensure that oxygen molecules occupy the majority of the surface vacancy sites of the ZnO NWs. The DC measurements show that the threshold voltage shifted from 0.05 in the vacuum to 0.87 V under the oxygen environment. This observation agrees with previously published reports that showed ZnO NW FETs' oxygen sensing properties. It has been proposed that O_2 molecules can be absorbed at surface vacancy sites of the metal-oxide nanowires and then accept electrons to form O_2^-. These chemisorbed O_2^- lead to the observed threshold voltage shift and deplete surface electron states; thus, at a given voltage, the channel carrier concentration is reduced and there is an accompanying decrease of the conductivity. Due to the threshold voltage shift, the carrier concentration in the channel has been reduced from 5.2×10^7 cm^{-1} (under vacuum) to 4.5×10^7 cm^{-1} (in dry O_2) at a gate bias of 6 V—if we assume that the average dielectric constant is the same for both cases. The mobility has also slightly decreased by ~6%. Figure 3 shows the device

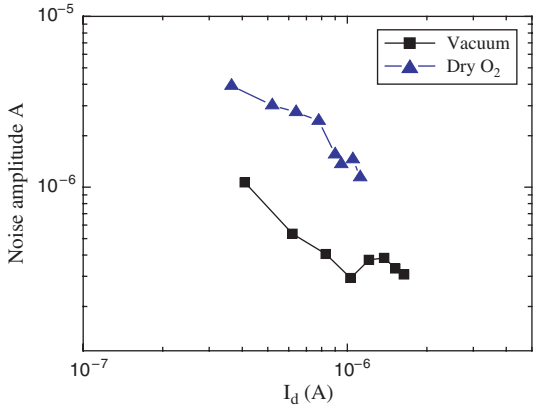

Fig. 3. Noise amplitude as a function of drain current under different gate biases in vacuum and the oxygen environments. $V_d = 1$ V.

noise amplitude as a function of drain current at various gate biases under different environments. As it reveals, the device noise level in the dry oxygen environment is nearly an order of a magnitude larger than that in vacuum. Measurements of the ZnO NW FETs in dry nitrogen environment did not show significant noise amplitude change compared to the vacuum data. The higher noise level in the oxygen environment can be elucidated by considering Hooge's empirical law $A = \alpha_H/N$. A similar fit to the oxygen noise data according to Eq. (3) gives a Hooge's constant of 4×10^{-2} for ZnO NW FETs under the oxygen environment. Compared to the observed α_H of 5×10^{-3} in vacuum, α_H in the oxygen environment is almost 8 time larger. We propose that the microscopically dynamic impact of the surface bound O_2^- species on the charge transport significantly increased the carrier number fluctuations related to electron trapping/detrapping events and accompanied scattering fluctuations in the device channel, which was reflected as an increased Hooge's constant under the oxygen environment. This is similar to the situation in traditional planar MOSFET devices, where the increase of fixed charges by, for example, bias stressing or ionizing irradiation results in a shift of threshold voltage and an elevated noise level.[11] The interactions between the O_2^- species and carriers increased both number fluctuations and mobility fluctuations in the channel, and therefore generated a larger noise amplitude for the ZnO NW FETs in the oxygen environment.

When the temperature is lowered to 4.2 K, the low frequency noise in the same device changes from $1/f$ type to a Lorentzian spectrum for another device with similar geometry, as shown in Figure 4, which has the form: $S_{I_{ds}}/I_{ds}^2 = A/(1 + f/f_c)^2$. The Lorentzian spectrum is caused by the trapping and detrapping of a single defect in the dielectric. The signature of this single trap state is shown in the RTS drain current of Figure 4 inset, where the current switches between two discrete channel current values. The corner frequency f_c can be estimated to be ~18 Hz by locating the peak of $S_{I_{ds}} * f$ versus f plot.

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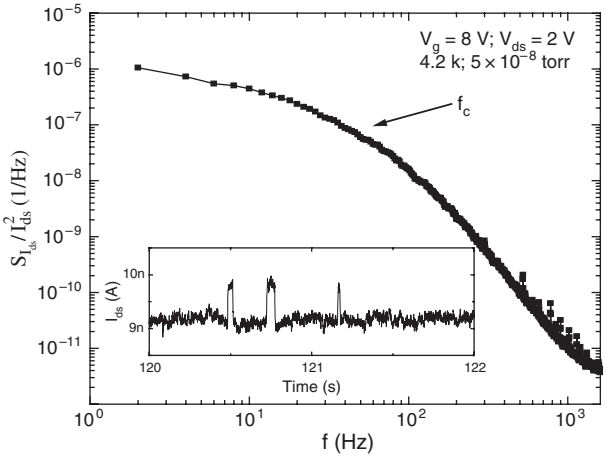

Fig. 4. Typical Lorentzian with corner frequency at ~18 Hz with the corresponding time-domain RTS in the inset.

This is consistent with the calculation from mean time at high current τ_{on} and low current τ_{off}, where $f_c = 1/2\pi\tau_0$ and $1/\tau_0 = 1/\tau_{on} + 1/\tau_{off}$. This observation indicates that the trapping/detrapping events are dominated by individual defects in the dielectrics and that RTS should be a huge concern for nanowire devices reliability, especially when the devices are scaled or when they are operated at low temperature.

4. CONCLUSIONS

In conclusion, we carried out noise characterizations of ZnO NW FETs and the obtained noise spectra displayed a classical $1/f$ frequency dependence. Examination of the gate dependence of the noise amplitude gave a Hooge's constant of 5×10^{-3} for the ZnO NW FETs, which is within the range of reported values of bulk materials or CMOS FETs with high-k dielectrics, supporting the feasibility of utilizing nanowires for future beyond-CMOS electronic applications. Measurements of the devices in dry O_2 environment exhibited a higher noise level, which could be attributed to the increased channel fluctuations associated with O_2^- bound at the ZnO surface. This study also suggests that the changes of the noise characteristics under different environments could be utilized as a new sensitive method for sensing applications. When temperature is reduced to 4.2 K, the noise spectra change from $1/f$ type to Lorentzian and the accompanying current traces show random telegraph signal signature, indicating the trapping/detrapping events caused by individual defects in the dielectrics.

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