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Fabrication, structural and electrical characterization of VO_2 nanowires

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Abstract

The structural and electrical properties of VO_2 nanowires synthesized on Si_3N_4/Si substrates or molybdenum grids by a catalyst-free vapour transport method were investigated. The grown VO_2 nanowires are single crystalline and rectangular-shaped with a preferential axial growth direction of [1 0 0], as examined with various structural analyses such as transmission electron microscopy, electron diffraction, X-ray diffraction, and X-ray photoelectron spectroscopy. In particular, it was found that growing VO_2 nanowires directly on Si_3N_4 deposited molybdenum transmission electron microscopy grids is advantageous for direct transmission electron microscopy and electron diffraction characterizations, because it does not involve a nanowire-detachment step from the substrates that may cause chemical residue contamination. In addition to structural analyses, VO_2 nanowires were also fabricated into field effect transistor devices to characterize their electrical properties. The transistor characteristics and metal–insulator transition effects of VO_2 nanowires were investigated.

Keywords: A. Nanostructures; A. Oxides; C. Electron microscopy

1. Introduction

Recently, nanowires have been extensively studied for the nanoscale electronic, magnetic, photonic and biological sensing device applications [1–8]. Unlike most semiconductor nanowire materials such as Si, GaAs, and GaN, metal oxide nanowires present an air-stable surface without the formation of an insulating native oxide layer, which can realize abrupt metal/semiconductor interfaces without any specific oxide-etching process [9]. Moreover, metal oxides have typically cations with mixed valence states and anions with vacancies, which provide the capacity for tunable electrical, optical, and chemical properties [10]. Various synthetic methods for growing nanowires of metal oxides such as ZnO, SnO_2, and Ga_2O_3 have been reported. These methods include vapour–liquid–solid (VLS) growth [11], vapour–solid growth by chemical vapour deposition [10], electrochemical deposition method in templates with porous anodic aluminium oxide [12], and solution growth [13].

Among these metal oxide materials, vanadium oxide compound materials have a unique electrical property in that some vanadium oxide compounds are known to undergo a metal–insulator transition (MIT). The transition

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Table 1
Summary of vanadium oxide compounds characteristics: the metal–insulator transition temperatures, crystal structures [13], and the reported binding energies for V $2p_{3/2}$ and O 1s [15]

Compounds	Transition temperature	Structure	V $2p_{3/2}$ (eV)	O 1s (eV)	ΔE (eV)
VO	Rise slowly with temperature	NaCl	–	–	–
VO_2	340 K	Rutile monoclinic → tetragonal	515.6	530.0	14.4
V_2O_3	150 K	Corundum	515.2	530.0	14.8
V_2O_5	–	Orthorhombic	516.9	529.8	12.8
V_3O_5	No transition	Rutile monoclinic	–	–	–

Properties unavailable are left blank in this table.

temperature of MIT effect varies for different oxygen content ratios among vanadium oxide compounds. For example, the transition temperature for divanadium trioxide (V_2O_3) is −127 °C, for vanadium dioxide (VO_2) is 67 °C whereas trivanadium pentoxide (V_3O_5) does not have a transition effect (Table 1) [14–17]. Among these, VO_2 has a MIT transition temperature closest to room temperature, thus, has been the most intriguing of these materials for use in device applications [20,21]. VO_2 is an insulator (or semiconductor) with a monoclinic structure below the MIT transition temperature, and after this temperature it exhibits an abrupt change in resistivity, becomes metallic, and transforms into a tetragonal structure [18]. Additionally, the optical properties of VO_2 materials change from infrared transmission to infrared reflection beyond the transition temperature [19]. With these dramatic changes in the physical and electrical properties, VO_2 materials have typically been used as Mott field effect transistors and thermochromic devices [19–21].

In this paper, we report on our experimental study on the synthesis and structural and electrical characterization of single crystalline VO_2 nanowires. Common VLS or vapour–solid–solid (VSS) growth techniques are used for synthesizing nanowires. Metal catalysts are typically incorporated in nanowire materials and may act as unintentional doping agents [22]. For this reason, VO_2 nanowires were synthesized in this study by a thermal vapour transport method without using any metal catalysts, a method initially proposed by Guiton et al. [2]. Recently, Sohn et al. also successfully synthesized epitaxially orientation-controlled VO_2 nanowires using a similar growth technique [23]. Our study reliably produced VO_2 nanowires with 10–100 of nanometres in diameter/size and a few microns in length on Si_3N_4/Si substrates, or Si_3N_4 deposited molybdenum transmission electron microscope (TEM) grids. In fact, nanowires grown directly on molybdenum TEM grids enable a simple and direct TEM characterization of nanowires since it does not involve a process such as sonication in a solution, as is necessary to detach nanowires from substrates to place on a TEM grid. The structural information of the VO_2 nanowires was studied with various analytic techniques such as TEM, electron diffraction, X-ray diffraction, and X-ray photoelectron spectroscopy. Also, to investigate the electrical properties of VO_2 nanowires, especially the MIT effect or transistor characteristics, individual VO_2 nanowires were fabricated as FET device structures and were subsequently characterized.

2. Experimental

VO_2 nanowires were grown by a vapour transport method without using any metal catalysts, previously reported by Guiton et al. [2]. Fig. 1(a) shows the schematic diagram of the set-up used in the nanowire synthesis. In this study, nanowires were grown either on silicon substrates or molybdenum TEM grids coated with 2000–3000 Å thick Si_3N_4 by plasma enhanced chemical vapour deposition (PECVD). Prior to silicon nitride deposition, each substrate was cleaned in acetone, methanol, and DI water for 5 min sonication. Substrates or TEM grids were then loaded into a quartz tube in a furnace (Lindberg; single zone 1200 °C furnace) with the VO_2 sources (VO_2 powders; 99.999% from Alfa Aesar). After loading, the tube was sealed, pumped at <0.1 Torr, and purged with argon at ambient temperature, then heated to a growth temperature of 900–1000 °C. During the growth of nanowires, the pressure inside the tube was maintained at ∼10 Torr with an argon flow rate of ∼3 sccm, controlled with a mass flow controller (Kofloc model 3660) for a growth time of ∼5 h. After the growth period, the furnace was cooled naturally to room temperature in an argon flow.

The structure of VO_2 nanowires was analysed by scanning electron microscopy (SEM, Hitachi S-4700), TEMs (Leo Zeiss Inc. EM912 Ω at 120 kV and Philips CM 20T/STEM high-resolution TEM at 200 kV), electron diffraction, X-ray diffraction (XRD, Rigaku), and X-ray photoelectron spectroscopy (XPS, ESCALAB 250 XPS spectrometer).

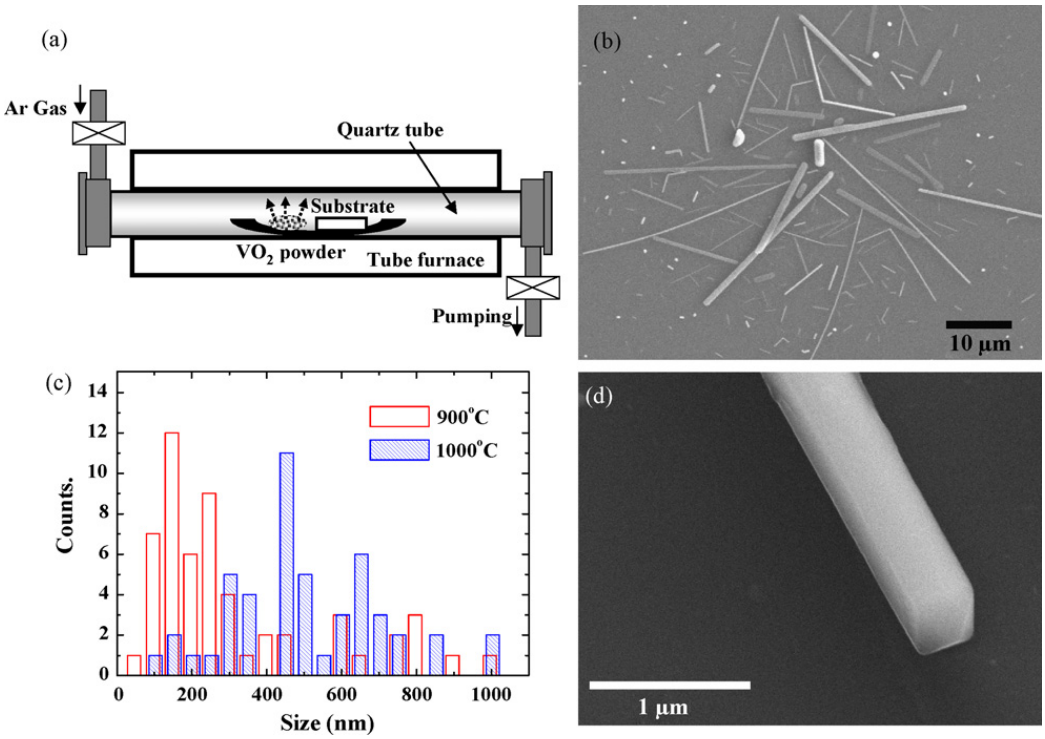

Fig. 1. (a) Schematic diagram of nanowire growth reactor. (b) SEM image of VO_2 nanowires grown at 900 °C on Si_3N_4/Si substrate. (c) Histogram of size and length of the nanowires grown at 900 °C and 1000 °C. (d) SEM image showing nanowire in a rectangular shape.

To characterize the nanowires grown on the Si_3N_4/Si substrates with either TEM or other methods, or to apply the nanowires to electronic device structures such as FETs, the nanowires need to be removed from the substrates. For example, in TEM characterization, the nanowires grown on Si_3N_4/Si substrates were detached from the substrate surface by sonication in isopropyl alcohol. Then the nanowires suspended in isopropyl alcohol were cast on a standard TEM grid (copper grid with holy carbon film) for TEM characterization. As mentioned previously, VO_2 nanowires were also grown directly on Si_3N_4 deposited molybdenum TEM grids for easy and direct TEM or electron diffraction characterizations; this process does not require the nanowire-detachment step of sonication.

In addition to structural characterizations, VO_2 nanowires were fabricated into FET electronic device structures to study their electrical properties. To accomplish this, individual VO_2 nanowires suspended in isopropyl alcohol were dropped onto a 100 nm thick thermally-grown oxide on silicon. The silicon substrate was a highly doped p-type (~0.005 Ω-cm) substrate that could serve as a common back gate. The VO_2 nanowires dropped on these substrates were then dried in an oven for a few hours at a temperature above 60 °C, to remove any chemical residue. Metal electrodes consisting of Cr (5 nm)/Au (45 nm) were then deposited by an electron beam evaporator, and defined as the source and drain electrodes by photolithography and a lift-off process. A Cr/Au metallization was selected to contact nanowires, because this bilayer was reported to produce ohmic contacts in VO_2 thin films [20,21]. The distance between the source and drain electrode was 2–3 μm. Electrical properties such as source–drain current versus voltage characteristics as a function of gate voltage were measured using a semiconductor parameter analyser (HP4155C). Here, the gate voltage was applied through the highly doped silicon back gate. VO_2 nanowire FET devices were measured with a wafer probe station equipped with a hot chuck and temperature controller to vary the temperature.

3. Results and discussion

3.1. Synthesis and structural characterization of VO_2 nanowires

A representative morphology of the VO_2 nanowires grown on a Si_3N_4/Si substrate is shown in Fig. 1. As can be seen, the nanowires are in a rectangular shape (Fig. 1(d)) with 40–1000 nm in size and 3–50 μm in length (Fig. 1(b and c)). The dimension and density of nanowires tend to depend on the growth conditions. For example, nanowires grown

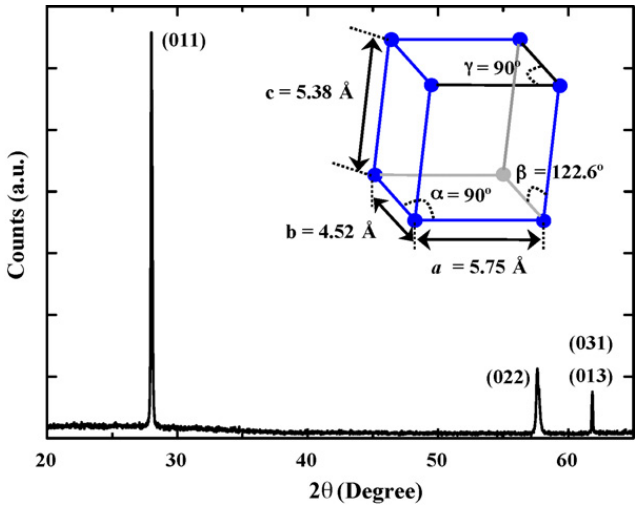

Fig. 2. XRD pattern of VO_2 nanowires. Inset is a schematic of a unit cell of VO_2 nanowires.

at higher temperature (1000 °C) are longer and thicker than those grown at lower temperatures (900 °C), as illustrated in the histograms in Fig. 1(c). This difference can be explained by the fact that a higher growth temperature generally increases low energy surface nucleation probability and supersaturation ratio via VO_2 powder evaporation, to the extent that denser and thicker nanowires will be grown at higher temperatures [2,10].

The structural properties of the grown VO_2 nanowires were characterized with various structural analyses such as SEM, TEM, electron diffraction, XRD, and XPS. Fig. 2 shows the XRD pattern of as-grown VO_2 nanowires, with Cu Kα radiation (λ = 1.542 Å) in a 40 V/40 mA condition. XRD spectra show the peaks (0 1 1), (0 2 2), (0 3 1), and (0 1 3), indicating that VO_2 nanowires are crystalline and have a preferred growth orientation. Also, these XRD peaks imply that the grown VO_2 nanowires are a monoclinic structure with lattice constants of $a = 5.75$ Å, $b = 4.52$ Å, $c = 5.38$ Å, and $\beta = 122.6$ ° (JCPDS Card no. 44-0252). The unit cell of a VO_2 nanowire is schematically illustrated in the inset of Fig. 2. It was determined that the monoclinic unit cell structure for the VO_2 nanowires is similar to that of VO_2 bulk materials, below the MIT temperature of 67 °C [13]. For more structural information, TEM and electron

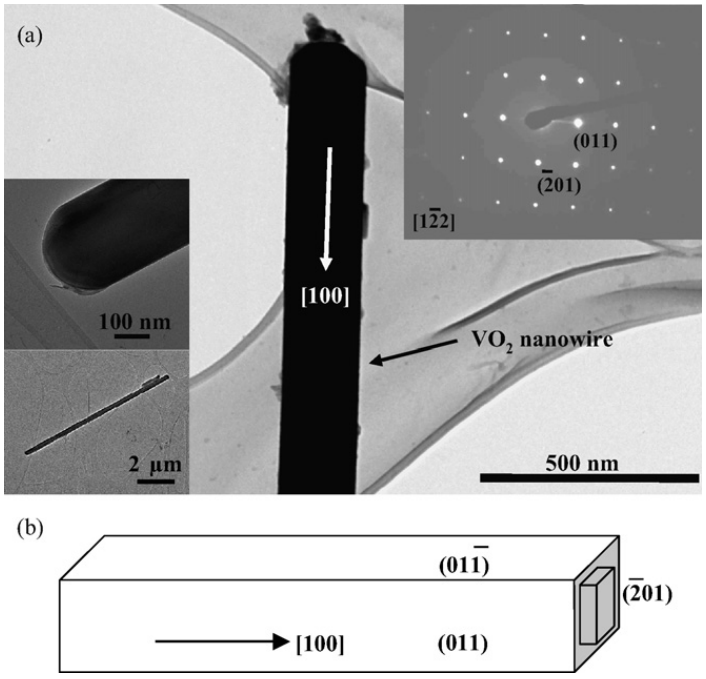

Fig. 3. (a) TEM images of a detached VO_2 nanowire. The insets are an electron diffraction pattern along the $[1\,\bar{2}\,2]$ zone axis and low-magnification TEM images of the growth front and the whole VO_2 nanowire. (b) The structure schematic of the grown VO_2 nanowire.

diffraction characterizations were carried out, and a TEM image of a single VO_2 nanowire is shown in Fig. 3 with an electron diffraction pattern in the inset of this figure. The electron diffraction pattern presents (0 1 1) and $(\bar{2}\,0\,1)$ diffraction spots, with a zone axis of $[1\,\bar{2}\,2]$, indicating a single crystal monoclinic VO_2 nanowire with an axial growth plane of $(\bar{2}\,0\,1)$ and growth axis in the [1 0 0] direction. From the data in Figs. 2 and 3(a), the structure of the rectangular-shaped VO_2 nanowires can be determined, as illustrated in Fig. 3(b). The top face of VO_2 nanowire is $(0\,1\,\bar{1})$ perpendicular to the electron beam in TEM characterization, the side surface is (0 1 1), and the axial growth plane is $(\bar{2}\,0\,1)$. Guiton et al. [2] have reported a similar crystal orientation of rectangular-shaped VO_2 nanowire. Although a comprehensive understanding of the VO_2 nanowire growth mechanism is still unknown, the intrinsic rectangular-faceted shape (not cylindrical), and the [1 0 0] growth direction of the VO_2 nanowires may be related to crystal plane dependent surface energy [2,10], as a low index plane generally has a lower surface energy. VO_2 nanowire growth in vapour transport method without metal catalyst may be also governed vapour–solid mechanism as reported in ZnO nanobelt growth mechanism without metal catalyst [10]. When VO_2 bulk source material is evaporated at high temperature, the part of vapour is condensed on the substrate for minimizing surface energy. After nucleating small particle, newly vaporized VO_2 atoms will keep depositing on nucleus. At 900–1000 °C growth temperature, mobile VO_2 atoms tend to be flat in the low energy surfaces, suppressing accumulation VO_2 vapour on this surface. More VO_2 vapour may stay on rough nanowire tip at lower energy sites, resulting in this nanowire growth. Fig. 3(a) inset shows tip of VO_2 nanowire with a round shape. Round-shaped nanowire tip indicates presence of steps, kinks with atomic scale roughness.

As mentioned above, MIT temperatures vary for different oxygen content ratios in vanadium oxide compound materials. For this reason, before we could investigate the electrical properties of MIT behaviours of VO_2 nanowires, we performed XPS experiments on VO_2 nanowires grown on Si_3N_4/Si substrates, the results of which are shown in Fig. 4. It was found that the binding energies of O 1s, V $2p_{1/2}$, and V $2p_{3/2}$ levels were 528.0, 521.2, and 513.6 eV, respectively. Moreover, it can also bee seen that the difference in binding energies (ΔE) between the O 1s and V $2p_{3/2}$ levels also vary for different oxygen content ratios in vanadium oxide compounds, as summarized in Table 1. For example, ΔE for V_2O_3 is 14.8 eV (O 1s: 530.0 and V $2p_{3/2}$: 515.2 eV), ΔE for V_2O_5 is 12.8 eV (O 1s: 529.8 and V $2p_{3/2}$: 517.0 eV), and ΔE for VO_2 is 14.3 eV (O 1s: 530.0 and V $2p_{3/2}$: 515.6 eV) [16]. The binding energies of vanadium oxide compounds are calibrated typically based on the O 1s peak position (530.0 eV) [16], then our observed values become 530.0, 523.2, and 515.6 eV for O 1s, V $2p_{1/2}$, and V $2p_{3/2}$ levels, respectively with ΔE = 14.4 eV. The comparison of binding energies and ΔE value indicates that the nanowires grown in our study are indeed close to VO_2 materials.

For TEM characterization (Fig. 3), the nanowires should be removed from the Si_3N_4 substrates in order to be placed on a TEM grid. As explained in the experimental section, this process typically involves a sonication step; isopropyl alcohol sonication in our study. This process has a drawback because nanowires are detached from the Si_3N_4 substrates with a relatively low yield, and there is an increased potential of contamination due to isopropyl alcohol residue around the nanowires. To prevent this drawback, a process that does not require the nanowire-detachment step was developed for TEM characterization. This new process is schematically explained in Fig. 5(a). As a brief explanation, starting

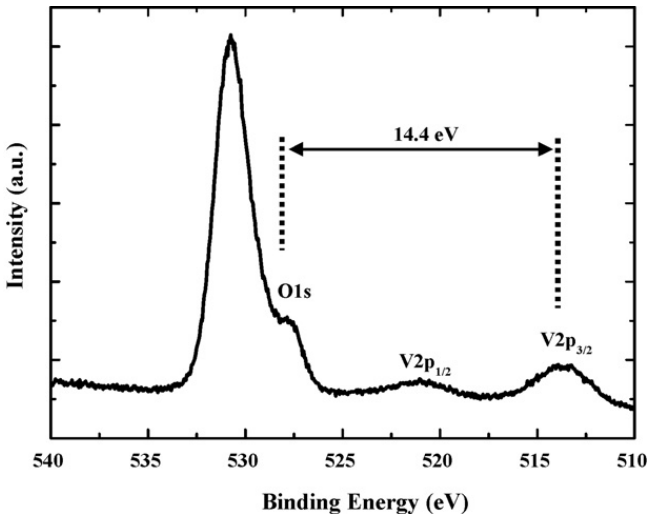

Fig. 4. XPS data of O 1s and V 2p spectra in VO_2 nanowires grown on Si_3N_4/Si substrate.

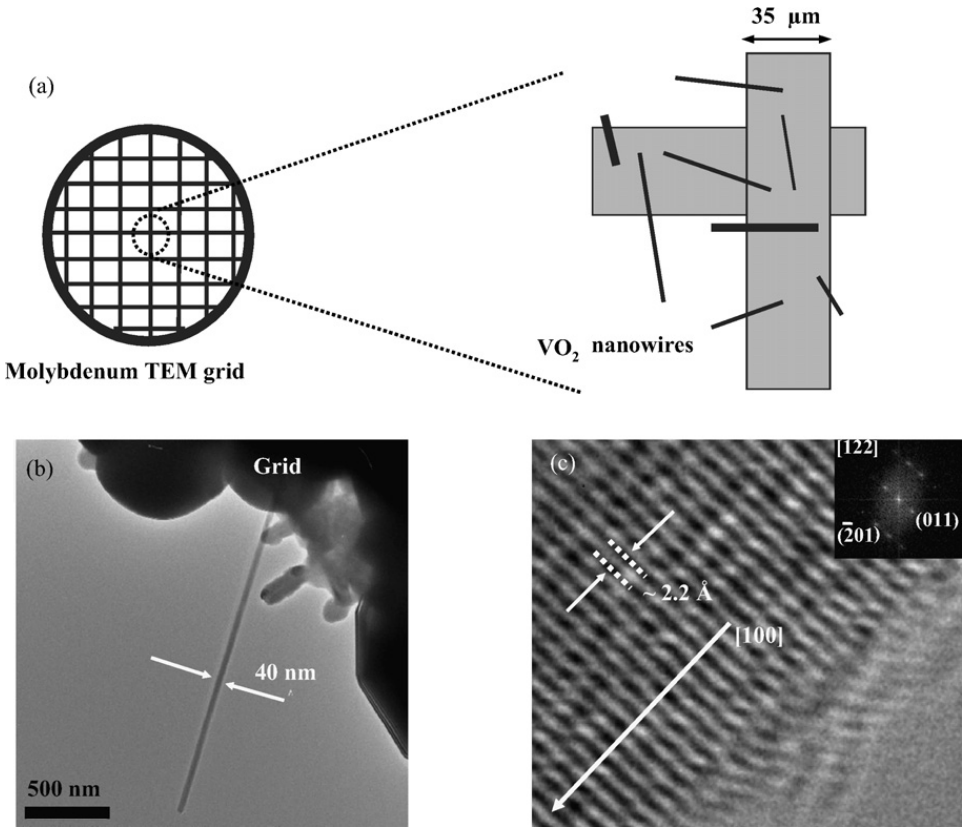

Fig. 5. (a) Schematics illustrating growth of VO_2 nanowires on Si_3N_4 deposited molybdenum TEM grid. (b) TEM image of VO_2 nanowire ~40 nm in size. (c) HRTEM image of a nanowire with a fast Fourier transform image (inset). Interplanar lattice spacing is 2.2 Å in $(\bar{2}\,0\,1)$ planes.

with molybdenum 200 mesh TEM grids deposited with 2000–3000 Å Si_3N_4 by PECVD, VO_2 nanowires were grown directly on the TEM grids. We used molybdenum grids because molybdenum has a high melting temperature (2623 °C). Fig. 5(b and c) shows TEM images of directly grown VO_2 nanowire on a molybdenum TEM grid. The nanowire in this figure is 40 nm in size. Fig. 5(c) is a high-resolution TEM (HRTEM) image with the fast Fourier transform image (inset). From this HRTEM image, the interplanar *d*-spacing of the VO_2 nanowire was observed as ~2.2 ± 0.3 Å which corresponds to the $(\bar{2}\,0\,1)$ lattice interplanar spacing of monoclinic VO_2 materials. We can calculate $(\bar{2}\,0\,1)$ lattice interplanar spacing with the interplanar spacing equation by using the lattice parameters obtained from the XRD characterization (Fig. 2) [24], as

$$\frac{1}{d^2} = \frac{1}{a^2}\frac{h^2}{\sin^2\beta} + \frac{1}{b^2}k^2 + \frac{1}{c^2}\frac{l^2}{\sin^2\beta} - \frac{2hl\cos\beta}{ac\sin^2\beta} \quad (1)$$

where *d* is (*h k l*) interplanar spacing, $a = 5.75$ Å, $b = 4.52$ Å, $c = 5.38$ Å, and $\beta = 122.6°$ (see the unit cell structure in the inset of Fig. 2). From the above equation, $(\bar{2}\,0\,1)$ lattice interplanar spacing can be calculated as 2.8 Å. The slight difference of the $(\bar{2}\,0\,1)$ interplanar spacing of VO_2 nanowires grown on two substrate types, i.e., nanowires grown on Si_3N_4/Si substrate (2.8 Å) and nanowires grown on molybdenum TEM grid (2.2 ± 0.3 Å) means that the structures of the VO_2 nanowires grown on the two substrates types are very similar although not exactly same. This can be due to a thermal mismatch between VO_2 nanowire and the surface of substrate, i.e., VO_2 and Si_3N_4/Si substrate versus free standing VO_2 nanowires. Note that the nanowires should be detached from TEM grids for the electrical characterization unless one can connect electrical leads directly to the nanowires on TEM grids.

3.2. Electrical characterization of VO_2 nanowires

In addition to the structural properties of VO_2 nanowires, the electrical properties of VO_2 nanowires were also studied. For the electrical characterization, VO_2 nanowires were detached from the Si_3N_4/Si substrate and transferred onto electronic device structures such as FETs. A SEM image of a VO_2 nanowire electronic device is shown in the

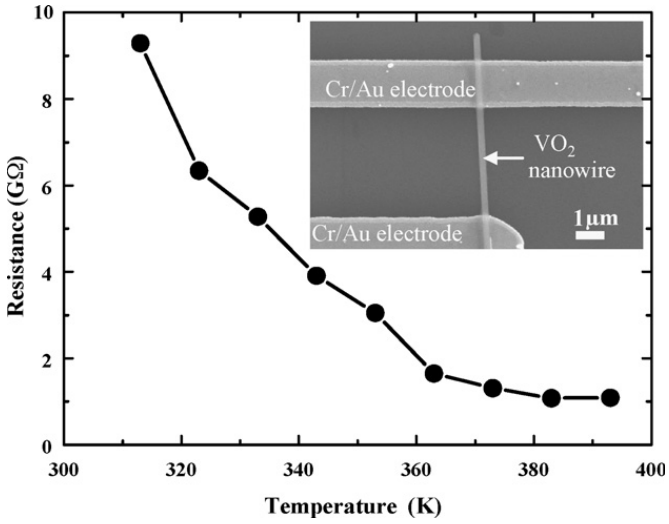

Fig. 6. Resistance of VO_2 nanowire as a function of temperature. Inset shows SEM image of a VO_2 nanowire electronic device.

inset of Fig. 6. As mentioned previously, VO_2 material is known to show a metal–insulator transition (MIT) effect around 67 °C (340 K). Fig. 6 is a plot of resistance measured from current–voltage characteristics as a function of temperature from 300 to 400 K. Here, the resistance was obtained from linear fitting from 0 to 2 V range. Due to short nanowire length, the resistance was measured in two point measurements. Unfortunately, this two point measured values were included contact resistance. Unlike typical VO_2 bulk materials [14,20], the MIT transition effect observed in the VO_2 nanowire device was not abrupt, but rather somewhat gradual in the measured temperature range. This gradual MIT behaviour has recently been reported, and is presumably due to an adhesive interaction between the VO_2 nanowire and the substrate causing a strain on the nanowire [25], or a local deviation of the oxygen content ratios in VO_2 nanowire [18].

The transistor characteristics of the individual VO_2 nanowire FET devices were also studied. Fig. 7(a) shows a source–drain current versus voltage (I_{sd}–V_{sd}) data from a single VO_2 nanowire FET at a range of gate voltages from −40 to 20 V, with 10 V increments. Additionally, Fig. 7(b) shows a source–drain current versus gate voltage (I_{sd}–V_g) for a fixed source–drain voltage of 5 V. It can be seen that the VO_2 nanowire FET displayed n-type semiconducting behaviour, since the current increases with increasing gate bias. Previous reports have indicated that electrons are major carriers with charge density of $\sim 10^{18}$ cm^{-3} and mobility ranging from 0.07 to 0.4 cm^2/V s in VO_2 thin films at room temperature [26–28]. The n-type behaviour of VO_2 nanowire has been explained due to the hopping transport among localized levels [29]. From the transistor data of VO_2 nanowire FET at room temperature (Fig. 7), we can calculate the electron carrier concentration n and carrier mobility μ. The electron charge carrier density can be estimated from $n = Q/ed^2L$, where $Q = CV_{th}$ (V_{th} is the threshold voltage), the capacitance $C = 2\pi\varepsilon\varepsilon_0 L/(\cosh^{-1}(1 + t/d))$ by assuming a cylindrical-shaped nanowire, t is the SiO_2 layer thickness (100 nm), d the nanowire side length (∼200 nm) and L is the nanowire channel

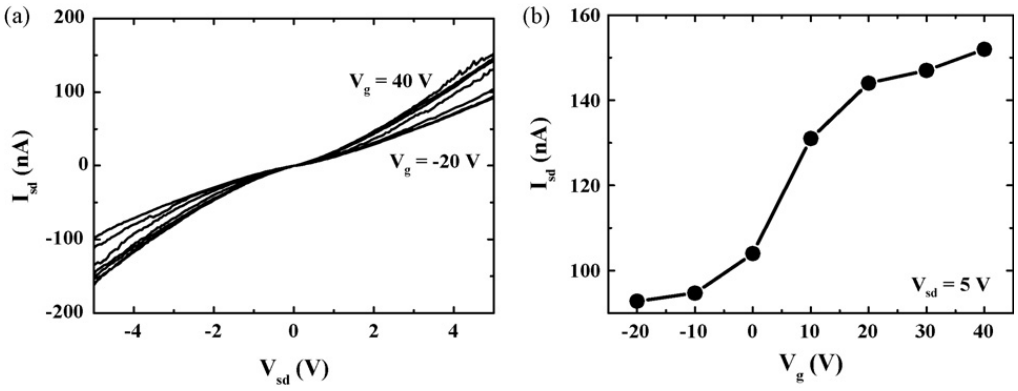

Fig. 7. (a) I_{sd}–V_{sd} plot for different gate biases from −40 to 20 V with 10 V increments for a VO_2 nanowire device. (b) I_{sd}–V_g plot at a fixed V_{sd} = 5 V.

length [30]. In this way, we estimated that $n \sim 10^{17}$ cm^{-3}. Additionally, the mobility μ can be calculated from $\mu = ((C/L^2)V_{sd})^{-1}(dI_{sd}/dV_g)$ and was found to be $\sim$0.2 cm^2/V s. Note that both carrier concentration and mobility of VO_2 nanowire measured in our study were determined to be similar those observed for VO_2 thin films [26–28], which suggests VO_2 nanowire "bulk" properties are dominant in the VO_2 nanowires.

4. Conclusion

VO_2 nanowires were successfully grown on a silicon substrate or molybdenum TEM grids by a catalyst-free method. From various structural analyses, the grown VO_2 nanowires were determined to be a rectangular-shaped monoclinic crystal structure with a preferential axial growth direction of [1 0 0]. The VO_2 nanowires grown directly on molybdenum TEM grids did not require a nanowire-detachment step from the substrates, thereby enabling a direct TEM characterization. Additionally, VO_2 nanowire field effect transistor devices were fabricated to study their electrical properties. A gradual metal–insulator transition effect was observed around 340 K, and transistor parameters such as carrier density and carrier mobility could be extracted.

Acknowledgements

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