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Tunable Electronic Transport Characteristics of Surface-Architecture-Controlled ZnO Nanowire Field Effect Transistors

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ABSTRACT

Surface-architecture-controlled ZnO nanowires were grown using a vapor transport method on various ZnO buffer film coated c-plane sapphire substrates with or without Au catalysts. The ZnO nanowires that were grown showed two different types of geometric properties: corrugated ZnO nanowires having a relatively smaller diameter and a strong deep-level emission photoluminescence (PL) peak and smooth ZnO nanowires having a relatively larger diameter and a weak deep-level emission PL peak. The surface morphology and size-dependent tunable electronic transport properties of the ZnO nanowires were characterized using a nanowire field effect transistor (FET) device structure. The FETs made from smooth ZnO nanowires with a larger diameter exhibited negative threshold voltages, indicating n-channel depletion-mode behavior, whereas those made from corrugated ZnO nanowires with a smaller diameter had positive threshold voltages, indicating n-channel enhancement-mode behavior.

One-dimensional nanostructures such as semiconducting nanowires or carbon nanotubes are promising materials for future nanoelectronic device applications. Among these, ZnO nanostructures have attracted considerable attention due to their direct wide band gap (~3.4 eV), large exciton binding energy (60 meV), and potential use in versatile applications such as field effect transistors (FETs),[1] chemical and biological sensing,[1,2] light-emitting devices,[3] and solar cells.[4] Nanowire FETs are the fundamental element among these nanoelectronic device applications; thus it is essential to understand the electronic transport properties of nanowire transistors.

In particular, it is well-known that interface roughness plays an important role in electronic transport for conventional metal−oxide−semiconductor field effect transistors (MOSFETs) and thin film transistors (TFTs).[5,6] Similarly, the electronic transport in nanowire transistors can be influenced by the surface morphology of nanowires associated with the interface roughness, including the presence of surface trap states at the interfaces between the nanowires and the dielectric layers of nanowire FETs.[7,8] In addition, the properties of nanostructures used as building blocks for the assembly of nanoscale devices strongly depend on their size and shape.[9] Therefore, the synthesis of surface morphology- and size-controlled nanostructures facilitates the fabrication and fundamental study of nanoscale devices with unique electrical properties.

Recently, zigzag-shaped and/or corrugated-shaped one-dimensional (1D) nanostructures of GaN,[10] GaSe,[11] and ZnO[12] have been synthesized. For example, Zhou et al. and Nam et al. have synthesized 1D GaN nanostructures with zigzag shapes and corrugated shapes by a thermal reaction of gallium sources and ammonia, respectively, at an elevated temperature.[10] Also, Peng et al. have reported that GaSe nanowires exhibited a variety of morphologies including straight, zigzag, and saw-tooth shapes, which could be controlled by altering the growth temperature and time.[11] ZnO nanowires with corrugated shapes or zigzag shapes

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grown using a vapor technique have also been reported.[12] Although many studies have been carried out on the shape-controlled nanostructures,[10–12] such research has been focused only on the growth itself and growth mechanism as characterized by structural/optical observations. Moreover, despite many studies on charge transport in ZnO nanowires,[1b,13] the surface morphology- and size-dependent effects on the electronic transport of nanowires with corrugated shapes or zigzag shapes have rarely been reported. The surface morphology and size of nanowires are closely related to the surface states and/or surface defects;[14,15,21] thus, the electronic transport of nanowires can be strongly influenced by the surface effects due to such surface states and/or defects.[7,8,16] Therefore, optimum control of the density of surface states and/or defects is a crucial factor in various device applications. For example, we have previously reported that ZnO nanowire FETs with *n*-channel depletion-mode and enhancement-mode transistors can be realized due to the difference of surface states and/or defects induced by the surface morphology of ZnO nanowire side walls.[17] The realization of such nanowire transistors having different operational modes can lead to wide applications for the logic circuits.[17] Ultimately, ZnO nanowires must have electrical tunability by surface morphology and size control in order to achieve the potential applications of ZnO nanowire-based electronic devices.

In this Letter, we show that the density of surface states and/or defects can be experimentally controlled by the surface morphology- and size-controlled ZnO nanowires grown on various ZnO buffer film-coated c-plane sapphire (c-Al_2O_3) substrates. We present the tunable electronic transport characteristics of surface-architecture-controlled ZnO nanowire FETs and demonstrate that the electrical tunability is associated with the surface effects by surface states and/or defects as well as the nanowire diameter.

ZnO nanowires with smooth and corrugated surface morphology were grown on ZnO buffer film-coated c-plane sapphire substrates with or without Au catalysts by a vapor transport method. The growth of ZnO nanowires by the vapor transport method has been reported in detail elsewhere (see also the Supporting Information).[18] To control the surface morphology and size of the ZnO nanowires, three sets of sapphire substrates with ZnO buffer films were used: (1) an undoped ZnO film with Au catalyst (denoted as Au−ZnO film) or without Au catalyst (denoted as ZnO film), (2) a gallium-doped ZnO film with Au catalyst (denoted as Au−GZO film) or without Au catalyst (denoted as GZO film), (3) an aluminum-doped ZnO film with Au catalyst (denoted as Au−AZO film) or without Au catalyst (denoted as AZO film). Additionally, an Au-coated sapphire (denoted as Au−sapphire) substrate was also used for comparison with the ZnO buffer film-coated sapphire substrates. ZnO buffer films with approximately 1 μm thickness were grown on the sapphire substrates by a radio frequency (rf) sputtering system using a commercially sintered ZnO target, a Ga_2O_3 (1 wt %)-doped ZnO target, and an Al_2O_3 (1 wt %)-doped ZnO target. The Au thin film (~3 nm) was deposited on some substrates using an e-beam evaporator to form Au catalysts as universal catalysts for the growth of one-dimensional nanostructures.

The size, surface morphology, and crystal structure of the ZnO nanowires were characterized using field emission scanning electron microscopy (FESEM) and transmission electron microscopy (TEM). The photoluminescence (PL) mapping system (RPM2000 model, Accent Opt. Tech., U.K.) with a 325 nm He−Cd laser (4.6 mW) as an excitation source was used to study the optical properties of the ZnO nanowires at room temperature. In order to enable statistical descriptions of the electronic transport characteristics of surface-architecture-controlled ZnO nanowires, a total of 327 nanowire FET devices were fabricated and characterized (Figure 3, Figure S1 in the Supporting Information): 48 FETs of nanowires grown on Au−ZnO film, 41 FETs of nanowires grown on ZnO film, 54 FETs of nanowires grown on Au−GZO film, 55 FETs of nanowires grown on GZO film, 58 FETs of nanowires grown on Au−AZO film, 51 FETs of nanowires grown on AZO film, and 59 FETs of nanowires grown on the Au−sapphire substrate. A detailed description of the fabrication of ZnO nanowire FET devices has been reported elsewhere (see also the Supporting Information).[18] In particular, all the FET devices were passivated by poly(methyl methacrylate) (PMMA) to remove the influence of water or gas molecules in ambient air on ZnO nanowire FETs and to improve the FET performance by enhancing the gate-coupling effects.[17–19] The electronic transport characteristics of the ZnO nanowire FETs were investigated using a semiconductor parameter analyzer (HP4155C) at room temperature.

The TEM images of surface-architecture-controlled ZnO nanowires grown on various substrates are shown in Figure 1. The TEM images show two different types of ZnO nanowires, with a corrugated surface (Figure 1, panels a, b, c, and f) and with a smooth surface (Figure 1, panels d and e). The diameters of the ZnO nanowires were found to be 83.6 ± 1.4, 89.9 ± 1.3, 85.7 ± 1.4, 111.9 ± 1.7, 107.7 ± 1.5, 88.6 ± 2.4, and 112.8 ± 1.7 nm for the nanowires grown on Au−ZnO film, ZnO film, Au−GZO film, GZO film, Au−AZO film, AZO film, and Au−sapphire substrates, respectively. Here, the average diameters and the error values of each type of nanowires were determined statistically from FESEM images of roughly ~100 different nanowires grown on each different type of substrates; however FESEM images were not enough to resolve the roughness of corrugated nanowires. The degree of the roughness of the corrugated nanowires could be estimated from TEM images in the following two ways: (i) the "absolute" roughness, which can be defined as the difference of the arithmetic mean values of maximum and minimum diameters of the corrugated nanowires, and (ii) the "relative" roughness, which can be defined as the absolute roughness divided by the average diameters of the corrugated nanowires. In these ways, we found the absolute roughness and relative roughness as 6.4 nm and 7.7%, 6.6 nm and 7.3%, 7 nm and 8.2%, and 5.8 nm and 6.5% for the corrugated nanowires grown on Au−ZnO film, ZnO film, Au−GZO film, and AZO film, respectively.

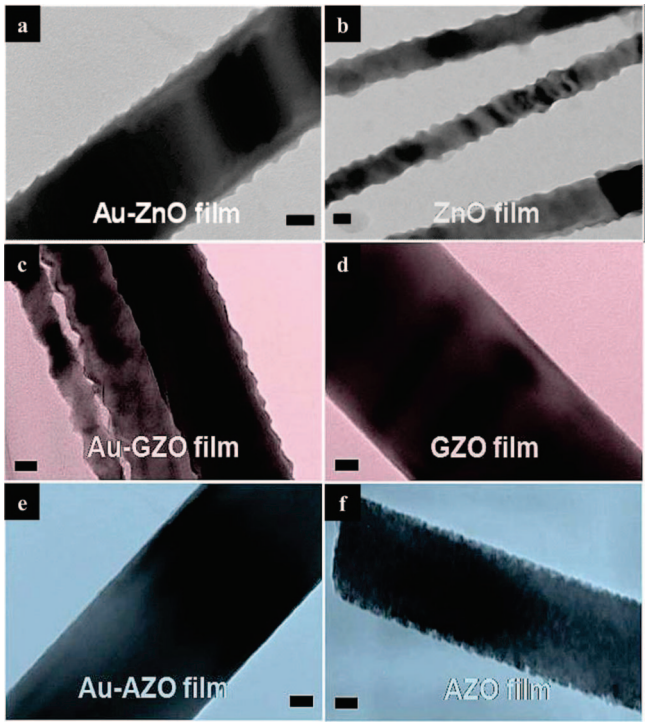

Figure 1. TEM images of the ZnO nanowires grown on various ZnO buffer film-coated c-plane sapphire substrates: undoped ZnO film (a and b), Ga-doped ZnO film (c and d), and Al-doped ZnO film (e and f) with and without Au catalysts, respectively. The scale bars are 20 nm.

As shown in Figure 1, the ZnO nanowires with relatively smaller diameters were found to have rougher surfaces than those with relatively larger diameters. The corrugated ZnO nanowires can have a larger surface area to volume ratio than smooth ZnO nanowires. These results indicate that the surface morphology and diameter size of the nanowire can be controlled by various substrates. Although the size-dependent growth mechanism of ZnO nanowires with corrugated and smooth surfaces grown on the different substrates is not yet clearly understood, we propose that ZnO nanowires with distinctive surface morphology and size can be formed due to various effects, which include nanocatalyst composition, interfacial layer, surface charge, surface roughness, surface strain, tensile stress, and Zn supersaturation variation.[11,20]

Panels a−f of Figure 2 show the PL spectra measured at room temperature for ZnO nanowires grown on various substrates. ZnO nanowires were first transferred from the growth substrates to silicon wafers, and the PL spectra were obtained from the ZnO nanowire transferred silicon wafers in order to eliminate signals coming from the ZnO buffer films themselves. The PL spectra in Figure 2 are the average values of individual signals acquired from 13 different positions within each ZnO nanowire transferred silicon wafer. As shown in Figure 2, the PL emissions of the ZnO nanowires consist of two main bands; one is the near-band-edge (NBE) excitonic related ultraviolet (UV) emission band with a peak position between 375 and 380 nm. The other is the broad deep-level (DL)-related emission (or trap-state emission) in the visible range that is attributed to the surface

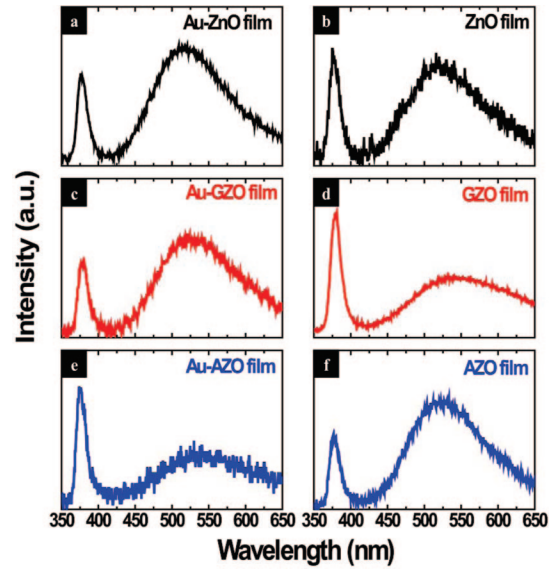

Figure 2. Photoluminescence spectra of the ZnO nanowires grown on various substrates.

defects of the crystal. Thus, DL emission is determined by the surface states and/or the concentration of the corresponding surface defects.[14,21] Although both the corrugated and smooth types of ZnO nanowires have both UV and DL emission peaks, the UV-to-DL emission ratios (I_{UV}/I_{DL}) are very different between corrugated and smooth ZnO nanowires. For the corrugated ZnO nanowires with relatively smaller diameters, the DL emission is strong and the UV emission becomes relatively weak, whereas for the smooth ZnO nanowires with relatively larger diameters, the DL emission is weak and the UV emission becomes relatively strong. Since the DL emission peak is a surface-related process, it reveals that the ZnO nanowires with large I_{UV}/I_{DL} ratios have a low density of surface states and/or defects, whereas those with small I_{UV}/I_{DL} ratios have a high density of surface states and/or defects.[14,21] Therefore, the luminescence of ZnO nanowires grown on various substrates is dependent on the surface morphology and the diameter size of nanowires, which play important roles in the process leading to visible emission. Although the origin of broad visible emission as typical characteristics of ZnO materials is still controversial, the surface states and/or defects are responsible for the surface morphology- and size-dependent luminescence.[14,21] These surface states and/or defects of ZnO materials introduce various defect energy levels inside the band gap of ZnO,[22] so that the surface effects by such surface states and/or defects influence the ZnO nanowire-based devices.

In order to study the influence of such surface states and/or defects on the electronic transport properties of surface-architecture-controlled ZnO nanowires, we have examined the electronic transport characteristics using the nanowire FET structure. Panels b−d of Figure 3 show the representative transfer characteristics, source−drain current versus gate voltage ($I_{DS}-V_G$) at a fixed source−drain voltage, $V_{DS} = 0.1$ V, of the surface-architecture-controlled ZnO nanowire FETs. The nanowires grown on different substrates exhibited

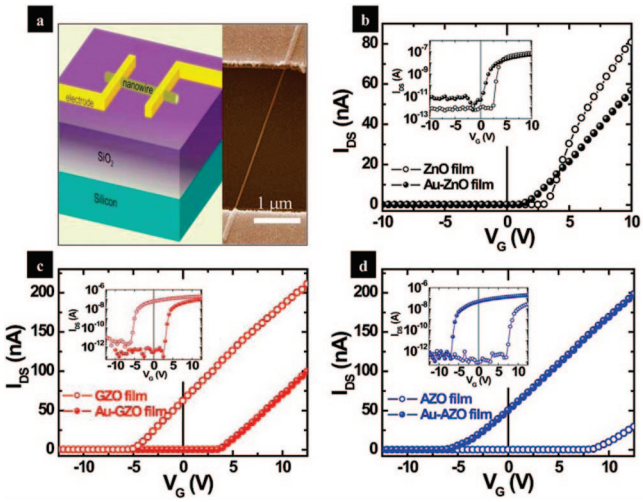

Figure 3. (a) Schematic diagram and SEM image of a ZnO nanowire FET. (b−-d) The $I_{DS}-V_G$ characteristics of FETs made from ZnO nanowires grown on various substrates, measured at V_{DS} = 0.1 V. Labels are explained in the text. The insets show the semilogarithmic plots of $I_{DS}-V_G$ curves with current on–off ratios as large as 10^4-10^6.

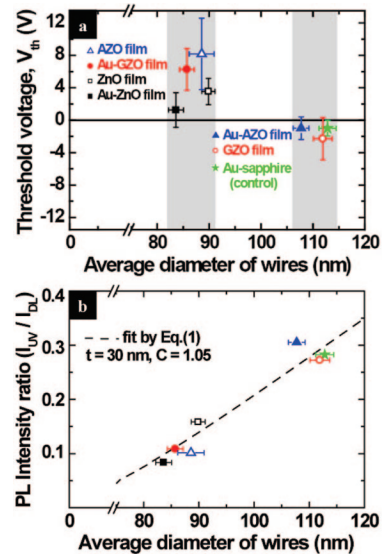

Figure 4. (a) Distribution of threshold voltages and (b) PL intensity I_{UV}/I_{DL} ratios with fitting curves as a function of the average diameter of ZnO nanowires.

different electronic transport characteristics. The FET devices made from smooth ZnO nanowires (nanowires grown on GZO and Au−AZO films; panels d and e of Figure 1) have negative threshold voltages (open symbols in Figure 3c and filled symbols in Figure 3d), indicating *n*-channel depletion-mode behavior that exhibits nonzero current at the zero gate bias. In contrast, the FETs made from corrugated ZnO nanowires (nanowires grown on Au−ZnO, ZnO, Au−GZO, and AZO films, Figure 1, panels a, b, c, and f) have positive threshold voltages (Figure 3b, filled symbols in Figure 3c, and open symbols in Figure 3d), indicating *n*-channel enhancement-mode behavior that exhibits off-current status at zero gate bias. The insets of panels b−d of Figure 3, the $I_{DS}-V_G$ plots on the semilogarithmic scale, display on/off current ratios as large as 10^5-10^6. Furthermore, the effective carrier concentration can be estimated from the total charge, $Q_{tot} = C_G|V_G - V_{th}|$ in the nanowire, where C_G is the gate capacitance and V_{th} is the threshold voltage required to deplete the nanowire.[17] The carrier concentration, $n_e = Q_{tot}/e\pi r^2 L$, can also be determined, where r is the nanowire radius and L (~4 μm) is the nanowire channel length. At V_G = 10 V, the carrier concentrations of the representative FET devices (Figure 3, panels b−d) were estimated as 1.09×10^{18}, 7.82×10^{17}, 7.68×10^{17}, 1.21×10^{18}, 1.26×10^{18}, and 1.62×10^{17} cm^{-3} for nanowires grown on Au−ZnO, ZnO, Au−GZO, GZO, Au−AZO, and AZO films, respectively. In addition, the transconductances ($g_m = dI_{DS}/dV_G$, slopes in $I_{DS}-V_G$ plots in Figure 3) above threshold voltages for the corrugated nanowires are comparable with those of the smooth nanowires. As seen in Figure S4 in the Supporting Information, the transconductance does not quite depend on the nanowire diameter or nanowire roughness.

In order to investigate the practical tunability of electronic transport characteristics in the surface-architecture-controlled ZnO nanowire FETs, we statistically examined all 327 FETs of the ZnO nanowires grown on various substrates. The threshold voltages observed for all 327 FETs are summarized in Figure 4 (see also Figure S1 in the Supporting Information). As shown in Figure 4a, the corrugated ZnO nanowires have relatively smaller diameters and positive threshold voltages, whereas smooth ZnO nanowires have relatively larger diameters and negative threshold voltages. Note that the threshold voltage is defined as the gate voltage obtained by extrapolating the linear portion of the transfer characteristics ($I_{DS}-V_G$) from the point of maximum slope to zero drain current, in which the point of maximum slope is the point where transconductance ($g_m = dI_{DS}/dV_G$) is maximal.[23] The negative threshold voltage, exhibiting depletion-mode behavior, is attributed to delocalized electrons from shallow donors in the channel, whereas the positive threshold voltage, exhibiting enhancement-mode behavior, is attributed to deep traps in the channel or at the interface.[28] Therefore, the electronic transport properties of the smooth ZnO nanowires with larger diameters are quite different from those of the corrugated ZnO nanowires with smaller diameters due to the scattering or trapping of the conduction electrons at the interfaces and/or near the surface of the ZnO nanowire. In particular, corrugated ZnO nanowires with smaller diameters can have a more significant fraction of the electron depletion region in the nanowire channel due to electron traps. The results shown in Figure 4a indicate that the surface morphology and the diameter size of nanowires can have a significant effect on the electronic transport properties of nanowire-based devices.

Figure 4b shows the relationship between the I_{UV}/I_{DL} ratios of the PL spectra of the ZnO nanowires (obtained from Figure 2) and the nanowire diameter. Smooth ZnO nanowires with larger diameters exhibited larger I_{UV}/I_{DL} ratios than corrugated ZnO nanowires with smaller diameters. The PL spectra and the I_{UV}/I_{DL} ratios are influenced by the surface effects and the diameter size of nanowires.[14,21] The I_{UV}/I_{DL} ratios can be fitted using the surface-recombination-layer

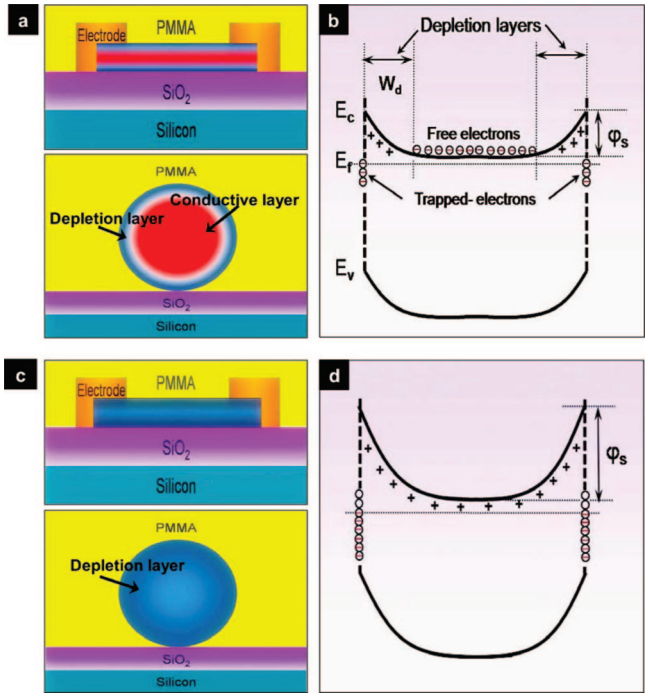

Figure 5. A cross-sectional view across the electrodes, ZnO nanowire, and dielectric layers (a and c) and the corresponding equilibrium energy band diagrams of nanowire FETs at $V_G = 0$ V (b and d) for smooth ZnO nanowires (a and b) and rough ZnO nanowires (c and d).

approximation model with the following equation[14]

$$\frac{I_{UV}}{I_{DL}} = C\left(\frac{(D/2)^2}{2(D/2)t - t^2} - 1\right) \quad (1)$$

where C is an approximation constant related to a collection efficiency difference at wavelengths of UV and DL peaks, D is the nanowire diameter, and t is a surface recombination thickness.[14] The thickness of the surface recombination layer (t) was assumed to be 30 nm as the previously reported value.[14,24] The optimized fitting curve obtained with eq 1 (using $t = 30$ nm, $C = 1.05$) is plotted as the dashed line in Figure 4b. This result implies that the contribution of the surface recombination to DL emission is predominant for smaller-diameter nanowires, resulting in increased surface effects.[14,21] Moreover, according to the analysis of X-ray absorption near-edge structure (XANES) spectra of the ZnO nanorods by Chiou et al.,[15a] the effect of surface states is enhanced when the diameter of ZnO nanorods is decreased. Therefore, tailoring the surface by controlling the surface morphology and diameter size of the nanowire plays an important role in the design and the fabrication of ZnO nanowire-based devices. Note that the difference in threshold voltage (ΔV_{th}) of various series of nanowire FET devices is correlated with the difference in I_{UV}/I_{DL} ratios ($\Delta(I_{UV}/I_{DL})$) observed for ZnO nanowires grown on various substrates. For example, {ΔV_{th} and $\Delta(I_{UV}/I_{DL})$} values were found as 2.29 V and 0.075, 8.54 V and 0.164, and 9.16 V and 0.204 between the ZnO nanowires grown on the Au−ZnO and ZnO films, Au−GZO and GZO films, and Au−AZO and AZO films, respectively. As plotted in Figure S5 in the Supporting Information, the values of ΔV_{th} increase along with $\Delta(I_{UV}/I_{DL})$.

Figure 5 shows cross-sectional schematics (Figure 5a,c) across the electrodes, ZnO nanowire, and dielectric layers with the corresponding equilibrium energy band diagram (Figure 5b,d) of the ZnO nanowire FETs at $V_G = 0$ V. Panels a and b of Figure 5 show the case for smooth ZnO nanowires, and panels c and d of Figure 5 depict the case for corrugated ZnO nanowires. For polycrystalline semiconductor materials, band bending can occur mainly due to interfacial traps at the grain boundaries,[6,25] whereas for single crystalline semiconductor materials, band bending can occur at surfaces and/or interfaces such as semiconductor/dielectrics,[7] semiconductor/electrodes,[16b] semiconductor/electrolytes,[26] and semiconductor/chemisorbates.[27] Similarly, the surface states and/or defects on single crystalline nanowires can induce trap energy levels at the interfaces, resulting in band bending due to Fermi level pinning.[8,9b,16b,c] The carrier trap states at the interfaces are important in determining the operation modes of transistors.[28] The trapping of carrier electrons in the trap states can cause electron depletion in the channel, resulting in a gate threshold voltage shift and a conductance modulation.[13a,c,25] Correspondingly, the tunable electronic transport behavior between corrugated and smooth ZnO nanowires can be explained by considering the depletion of electron carriers due to surface band bending at the PMMA/ZnO nanowire and/or ZnO nanowire/SiO_2 interfaces as shown in Figure 5. Note that for convenience of discussion and simplification of charge transport mechanism, we assumed the uniform charge and gate potential distribution for nanowires with circular cross sections. However, the typical back-gate nanowire FET geometry is significantly influenced by the cross-sectional shapes of nanowires and whether the nanowire is embedded or not.[20a] In addition, the back-gate nanowire FET geometry has the limitation in accuracy for calculating the gate-nanowire capacitance as well as the complication for the experimental extraction of transport parameters under the presence of depletion region and trap states.[7,19b]

To confirm depletion by surface band bending, we can compare the geometrical diameter of the nanowire with the depletion region (W) considered effective diameter, which can be estimated as[1b,8,29]

$$W = \left(\frac{2\epsilon_{ZnO}\varphi_S}{eN_D}\right)^{1/2} \quad (2)$$

where φ_s is the surface barrier potential, e is the electronic charge, N_D is the doping density, and ϵ_{ZnO} is the dielectric constant of ZnO. Then by using the depletion approximation and charge neutrality condition,[25b,29] the surface trap density (N_t) can be estimated as $N_t = 2N_D W$. Thus, the effective diameter (D_{eff}) of the conduction layer in the nanowire channel can be expressed as

$$D_{eff} = D - \left(\frac{N_t}{N_D}\right) \quad (3)$$

where D is the geometrical diameter of nanowire. Therefore, by assuming that the $N_D = 10^{17}$ /cm^3, $\epsilon_{ZnO} = 8.66$,[30] $\varphi_S = 0.3$ eV, and the nanowire diameter (D) is 100 nm, we obtain $W = 54$ nm and $D < 2W$ from eqs 2 and 3 (see also Figure S3 in the Supporting Information). This result indicates that the surface depletion can have a significant influence on the electronic transport behavior of ZnO nanowires since the

depletion width can be comparable to the diameter size of nanowire. Therefore, smooth ZnO nanowires are partially depleted under the no gate bias condition due to the smaller depletion region than the nanowire diameter (Figure 5a,b), whereas corrugated ZnO nanowires are completely depleted under the no gate bias condition (Figure 5c,d) due to the larger depletion region than the nanowire diameter. This explains why the operation mode of ZnO nanowire FETs can be controlled by the modulation of surface states and/or defects by surface morphology and size control. Consequently, the smooth ZnO nanowire FETs with large diameters can operate as the *n*-channel depletion-mode type with a partially depleted channel region due to the low density of surface trap states (Figure 5a), whereas the corrugated ZnO nanowire FETs with small diameters can operate as the *n*-channel enhancement-mode type with a fully depleted channel region due to the high density of surface trap states (Figure 5b) under the no gate bias condition.

In summary, we have shown that surface states and/or defects can be controlled by altering the surface architecture of the ZnO nanowires grown on various ZnO buffer film-coated sapphire substrates through the vapor transport method. We have presented the tunable electronic transport characteristics of the surface-architecture-controlled ZnO nanowire FETs and demonstrated their surface morphology- and size-dependent electrical tunability attributable to surface effects and band bending at the interfaces between the ZnO nanowire and dielectric layer.

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Supporting Information Available: Descriptions of synthesis of ZnO nanowires and fabrication of ZnO nanowire FETs, statistical distribution of threshold voltages for ZnO nanowire FETs, characteristics of ZnO nanowires grown on an Au-coated sapphire substrate, depletion width and effective diameter of ZnO nanowires, and transconductance vs nanowire diameter or roughness, PL intensity ratio (I_{UV}/I_{DL}) vs threshold voltage. This material is available free of charge via the Internet at http://pubs.acs.org.

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