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Effects of surface roughness on the electrical characteristics of ZnO nanowire field effect transistors

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Abstract

We have systematically investigated the effects of surface roughness on the electrical characteristics of ZnO nanowire field effect transistors (FETs) before and after passivation by poly (methyl metahacrylate) (PMMA), a polymer-insulating layer. To control the surface morphology of ZnO nanowires, ZnO nanowires were grown by the vapor transport method on two different substrates, namely, an Au-catalyzed sapphire and an Au-catalyzed ZnO film/sapphire. ZnO nanowires grown on the Au-catalyzed sapphire substrate had smooth surfaces, whereas those grown on the Au-catalyzed ZnO film had rough surfaces. Electrical characteristics such as the threshold voltage shift and transconductance before and after passivation were strongly affected by the surface morphology of ZnO nanowires.

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Keywords: Surface roughness; Passivation; ZnO; Nanowire; Field effect transistor

1. Introduction

ZnO nanostructures have been extensively studied due to their unique physical properties of direct wide-band gap energy (3.37 eV) and large exciton binding energy (60 meV) as well as for their versatile applications in electronic and optoelectronic devices [1,2]. In recent years, a variety of nanodevices such as light-emitting diodes [3,4], logic circuits [5], transistors [6], photodetectors [7], chemical sensors [8,9], and solar cells [10] have been fabricated using ZnO nanowires. Since nanowire field effect transistors (FETs) are the fundamental building blocks in potential nanoelectronic device applications, they have been fabricated and extensively studied with a typical back-gate configuration employing a highly-doped Si substrate with a dielectric layer [5,6,11–13]. However, the back-gate ZnO nanowire FETs can easily be affected by the undesirable chemisorptions of ambient gases, primarily oxygen [12]. Thus, several works have been carried out to improve the performance of ZnO nanowire FETs by using back-gate geometry with passivation layer or top-gate geometry [12–14].

In addition, the surface roughness in nanowire transistors plays an important role in electron transport [15,16]. However, in spite of the extensive works on ZnO nanowire FETs [5,6,11–13], the effects of surface morphology on the electrical properties of ZnO nanowires before and after passivation have not been thoroughly investigated. Recently, ZnO nanowires with rough surface have been grown on Si substrate by a ball milling and annealing method, but the research has focused only on the growth and characterization of nanowires [17]. Very recently, we have reported PMMA-passivated ZnO nanowire FETs with different operation modes in which the FET devices using smooth ZnO nanowires exhibited depletion-mode (D-mode) behaviour, whereas those using rough ZnO nanowires exhibited enhancement-mode (E-mode) behaviour [6].

In this study, we systematically investigated the effects of surface roughness on the electrical characteristics of ZnO nanowire FETs before and after passivation. The results showed that the performance and characteristics of ZnO nanowire FETs were directly influenced by the surface roughness of ZnO nanowires which could induce the interface roughness at the

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electrodes/ZnO nanowire, the ZnO nanowire/SiO_2 layer, and the ZnO nanowire/polymer-insulating layer, acting as deep traps at the interfaces.

2. Experimental procedure

ZnO nanowires were grown vertically on the substrates by the vapor transport method. A detailed description of the growth of ZnO nanowires has been reported elsewhere [12]. To control the surface morphology of ZnO nanowires under same growth conditions (growth temperature = ~920 °C, growth time = ~20 min, and flow rate = Ar 50 sccm, O_2 0.2 sccm), we used two different substrates, namely, an Au-catalyzed sapphire substrate and an Au-catalyzed ZnO film/sapphire. Prior to the growth of ZnO nanowires, we prepared two different substrates as follows. First, a ZnO film (~1 μm thick) was grown on a *c*-plane sapphire (*c*-plane Al_2O_3) substrate by an RF sputtering system using a commercially sintered ZnO target. Then the Au thin film (~3 nm) was deposited on the ZnO film/*c*-plane sapphire substrate using an electron-beam evaporator. At the same time, the Au thin film was deposited directly on a c-plane sapphire substrate. The surface morphologies of the ZnO nanowires grown on these two different substrates were characterized by field emission scanning electron microscopy (FE-SEM) and transmission electron microscopy (TEM). The average diameters were found to be approximately 112 and 85 nm for the ZnO nanowires grown on the Au-catalyzed sapphire substrate and for those grown on the Au-catalyzed ZnO film, respectively. The growth direction for the two types of ZnO nanowires were found identical from FE-SEM and TEM study.

To investigate the effects of surface roughness on the electrical characteristics before and after passivation of the FET devices made from ZnO nanowires grown on two different substrates, we fabricated and measured 44 FET devices (22 FETs of ZnO nanowires grown on the Au-catalyzed sapphire substrate and 22 FETs of ZnO nanowires grown on the Au-catalyzed ZnO film). All of them were characterized before and after passivation by poly (methyl metahacrylate) (PMMA), which is a polymer-insulating layer as a lithographic resist [18]. A detailed description on the fabrication of ZnO nanowire FET devices has been reported elsewhere [12]. As shown in Fig. 1(c), the distance between source and drain electrodes was approximately 3–4 μm and the electrodes were formed by Ti (100 nm)/Au (100 nm). We then systematically measured the electrical characteristics of the FETs made from ZnO nanowires grown on the two different substrates before and after passivation by using a semiconductor parameter analyzer (HP4155C).

3. Results and discussion

Fig. 1(a) and (b) show the low resolution TEM images of the Au-catalyzed sapphire substrate and the Au-catalyzed ZnO film/sapphire substrate, respectively. As shown in the TEM images, the ZnO nanowires grown on the Au-catalyzed sapphire substrate had relatively smooth surfaces, whereas those grown on the Au-catalyzed ZnO film had rough surfaces. Fig. 1(c) and (d) show the schematic diagram and FE-SEM image of the ZnO nanowire FET with a back-gate configuration, respectively.

The electrical characteristics of the FET devices made from ZnO nanowires grown on the two different substrates before

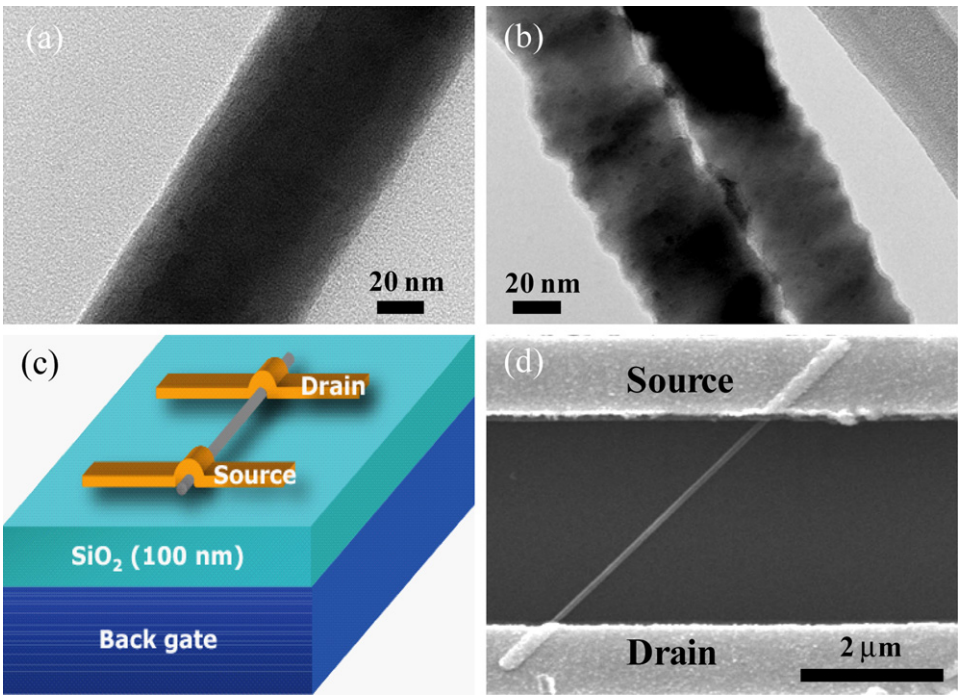

Fig. 1. Low resolution TEM images of the ZnO nanowires with smooth surface (a) and rough surface (b). (c) Schematic structure of a ZnO nanowire FET. (d) FE-SEM image of a ZnO nanowire FET.

and after passivation are summarized in Figs. 2 and 3. Fig. 2(a) and (b) show the representative output characteristics (source-drain current vs. voltages, I_{DS}–V_{DS}) and transfer characteristics (source-drain current vs. gate voltages, I_{DS}–V_G) for the FETs of smooth ZnO nanowires grown on the Au-catalyzed sapphire substrate. As shown in Fig. 2(a), the passivated FETs of smooth ZnO nanowires exhibited more well-defined saturation and pinch-off characteristics than the unpassivated devices. In particular, the decreasing separation between I_{DS} curves at larger currents before passivation is reflected in the output characteristics (I_{DS}–V_{DS}) (Fig. 2(a)), which is attributed to either an electron injection barrier at the source electrode or to mobility degradation associated with the interface roughness scattering of channel electrons at the channel/insulator interface with increasing gate voltage [19]. The I_{DS}–V_G curves in Fig. 2(b) show the threshold voltages (V_{th}) of −4.16 and −2.25 V before and after passivation, respectively. Note that the threshold voltage is defined as the gate voltage obtained by

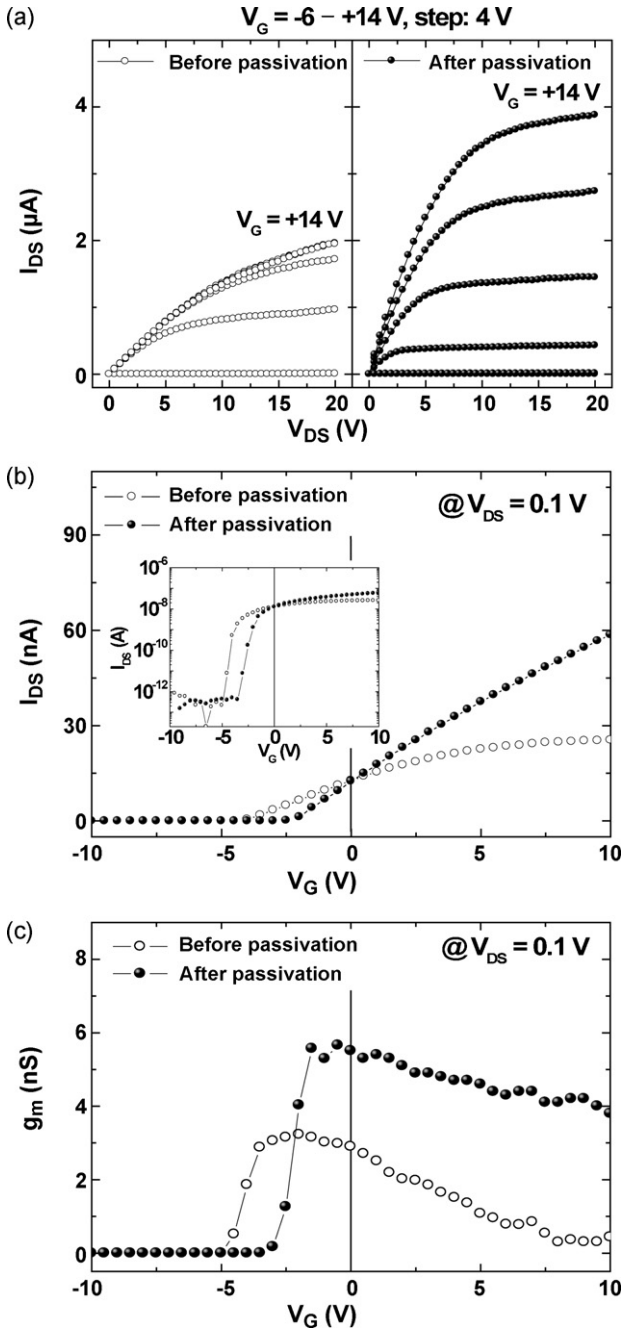

Fig. 2. The electrical characteristics of smooth ZnO nanowires grown on the Au-catalyzed sapphire substrate before and after passivation. (a) Ouput characteristics, (b) transfer characteristics, and (c) transconductance as a function of gate bias of a ZnO nanowire FET.

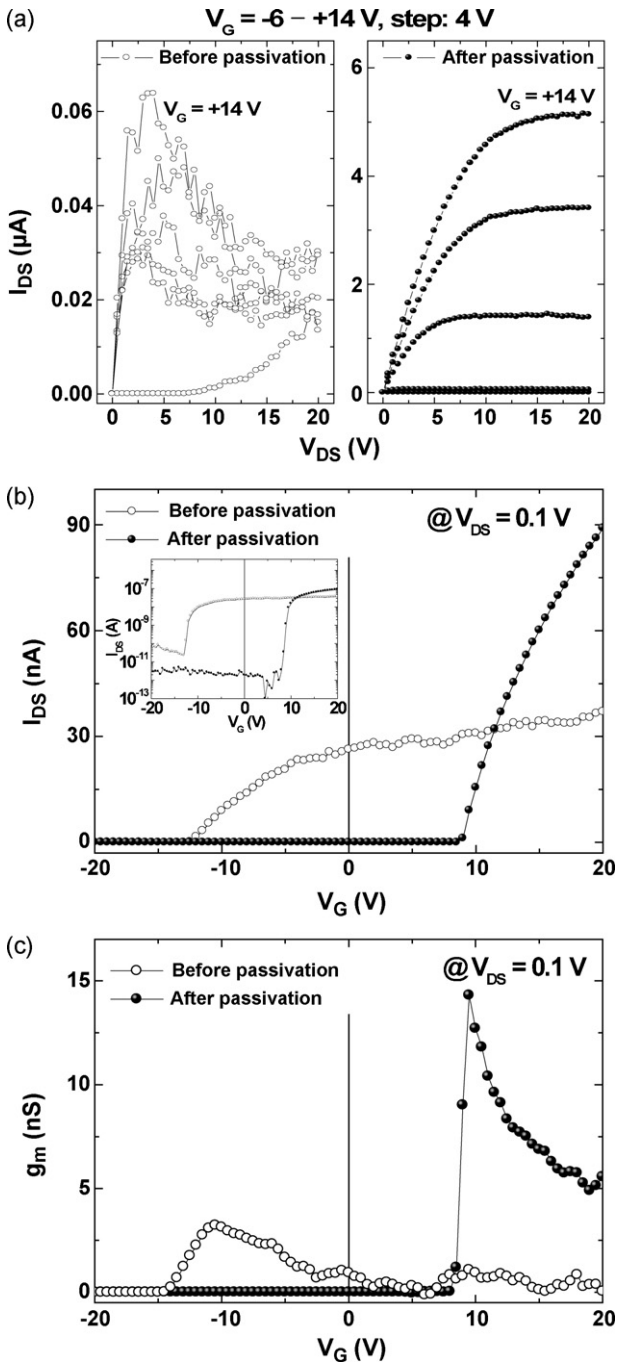

Fig. 3. The electrical characteristics of rough ZnO nanowires grown on the Au-catalyzed ZnO film before and after passivation. (a) Ouput characteristics, (b) transfer characteristics, and (c) transconductance as a function of gate bias of a ZnO nanowire FET.

extrapolating the linear portion of the transfer characteristics (I_{DS}–V_G) from the point of maximum slope to zero drain current, in which the point of maximum slope is the point where transconductance ($g_m = dI_{DS}/dV_G$) is maximum [20]. Although the I_{DS}–V_G curves in all the fabricated FET devices were not shown here, the threshold voltages after passivation shifted toward the negative gate bias direction for some devices and toward the positive gate bias direction for other devices. However, regardless of the threshold voltage shifts, most devices before and after passivation operated as *n*-channel depletion-mode (D-mode) behaviours, which exhibited negative threshold voltages and nonzero currents at zero gate bias. These results are consistent with the previous report in which the FET devices made from ZnO nanowires grown on an Au-coated sapphire substrate exhibited *n*-channel D-mode operation [6]. The current on/off ratios (I_{on}/I_{off}) before and after passivation for this FET device of smooth ZnO nanowire exhibit approximately 10^4–10^5 as shown in the inset of Fig. 2(b). Additionally, the maximum transconductance ($g_{m\ max}$) of the unpassivated FET is 3.2 nS, whereas $g_{m\ max}$ is 5.6 nS for the passivated FET (Fig. 2(c)). The carrier mobility (μ_e) in the low field region can be calculated by [12]:

$$\mu_e = \frac{dI_{DS}}{dV_G}\frac{L^2}{V_{DS}C_G} \quad (1)$$

where L is the nanowire channel length (≈4 μm), C_G the gate-nanowire capacitance, and $V_{DS} = 0.1$ V. The mobility of this smooth nanowire was found as ∼9.9 and ∼17.4 cm^2/Vs before and after passivation, respectively.

On the contrary, for the FET devices made from rough ZnO nanowires grown on the Au-catalyzed ZnO film, the unpassivated devices showed the poor electrical characteristics as shown in the output curves (I_{DS}–V_{DS}) (Fig. 3(a)), that is, the I_{DS} suddenly decreased with the further increase of V_{DS} and V_G beyond saturation. On the other hand, the passivated devices had well-defined linear regimes at low biases and saturation regimes at high biases as typical of transistors, indicating clear pinch-off behaviour. Unlike the FET devices made from smooth ZnO nanowires, the threshold voltage for the FET devices made from rough ZnO nanowires shifted toward the positive gate bias after passivation. The threshold voltage of the particular FET device shown in Fig. 3(b) shifts from −12.5 to +8.9 V, indicating transition from D-mode to E-mode operations (E-mode devices have positive threshold voltages and off current status at zero gate bias) [6]. Furthermore, as shown in the inset of Fig. 3(b) and (c), the unpassivated device exhibits I_{on}/I_{off} of 10^3–10^4 and $g_{m\ max}$ of 3.2 nS, whereas for the passivated device, I_{on}/I_{off} and $g_{m\ max}$ are 10^4–10^5 and 14.3 nS, respectively. The carrier mobility for this rough nanowire in the low field region before and after passivation was found as ∼11.1 and ∼49.5 cm^2/Vs, respectively. Similarly, compared with the characteristics of the passivated FET devices of smooth ZnO nanowires, most of the passivated FET devices of rough ZnO nanowires exhibited superior electrical performance than the unpassivated devices of rough ZnO nanowires, as shown in Fig. 3. These results are in good agreement with the superior characteristics of the ZnO nanowire FETs passivated by SiO_2/Si_3N_4 layer [13].

Fig. 4 shows the statistical results of the changes in the threshold voltages and the transconductances of ZnO nanowire FETs before and after passivation by PMMA. Fig. 4 also summarizes the electrical characteristics for 22 FET devices made from smooth ZnO nanowires and 22 FET devices made from rough ZnO nanowires. For the FETs of smooth ZnO nanowires, the average shift in threshold voltage (ΔV_{th}) is around 6.7 V, whereas the average ΔV_{th} for those of rough ZnO nanowires is 21.7 V as shown in Fig. 4(a). The threshold voltages of the two different groups of smooth and rough ZnO nanowires shifted toward the positive gate bias direction, implying a formation of surface depletion layer due to the presence of surface charge traps of the ZnO nanowire [21,22]. However, if the surface of the ZnO nanowires is highly smooth and well passivated, the threshold voltage may shift toward the negative gate bias direction due to the removal of the chemisorptions of O_2 molecules [23,24]. In particular, the FETs of rough ZnO nanowires showed the D-mode behaviours before passivation and E-mode behaviours after passivation. Furthermore, the changes in the threshold voltages for the rough ZnO nanowires were much larger than those for the smooth ZnO

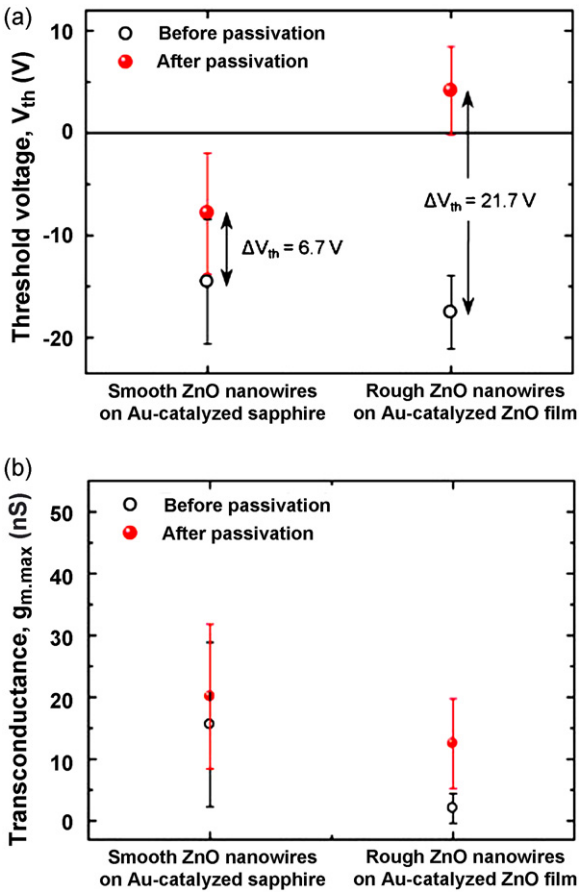

Fig. 4. Comparison of threshold voltage (V_{th}) (a) and maximum transconductance ($g_{m\ max}$) (b) of the FETs made from smooth and rough nanowires before and after passivation. Total 44 ZnO nanowire FET devices were fabricated and measured (22 FETs of smooth ZnO nanowires and 22 FETs of rough ZnO nanowires).

nanowires. These results indicate that the surface roughness of ZnO nanowires cause the threshold voltage to shift toward the positive gate bias direction because the channel width is narrowed due to the formation of a depletion region by the trap of electrons at ZnO nanowire/SiO_2 and/or ZnO nanowire/PMMA interfaces. This is consistent with the shifts in the threshold voltage due to the channel narrowing effect by band bending at the interface of the Au/CdS nanobelt [25]. Fig. 4(b) shows the maximum transconductance $g_{m\,max}$ for all the fabricated FET devices. For the 22 FETs of smooth ZnO nanowires, $g_{m\,max}$ at $V_{DS} = 0.1$ V is 15.6 ± 13.3 and 20.13 ± 11.7 nS before and after passivation, respectively, and for the 22 FETs of rough ZnO nanowires, $g_{m\,max}$ at $V_{DS} = 0.1$ V is 2.05 ± 2.42 and 12.52 ± 7.25 nS before and after passivation, respectively. Thus, for the two different groups of ZnO nanowires as shown in Fig. 4(b), the FETs exhibited more efficient gating effects after passivation, which is consistent with the electrical characteristics of top-gate ZnO nanorod MOSFETs [14]. Most of the unpassivated FET devices of the rough ZnO nanowires showed weaker gate dependence than those of the smooth ZnO nanowires, implying weaker electrostatic gating effects and much lower capacitances for the rough ZnO nanowires. The inferior electrical characteristics of the rough ZnO nanowire-based FETs without the passivation layer can also be due to the weak gate coupling caused by the physically poor contact between the nanowire and the SiO_2 layer. However, after passivation by the polymer-insulating layer, nanowires are embedded within the insulating layer, leading to the enhancement of the gating effects and transconductance.

Additionally, in typical back-gate-nanowire FET geometry, the transconductance g_m (dI_{DS}/dV_G) and gate-nanowire capacitance (C_G) are expressed as [14,26]:

$$\frac{dI_{DS}}{dV_G} = \mu_e \frac{V_{DS} C_G}{L^2} \tag{2}$$

$$C_G = \frac{2\pi\varepsilon_r\varepsilon_0 L}{\cosh^{-1}((r+h)/r)} \tag{3}$$

where μ_e is the electron mobility, h the gate oxide thickness (=100 nm), r the nanowire radius, and ε_r the dielectric constant of the gate insulating layer ($\varepsilon_r = 3.9$ for SiO_2), and ε_0 the permittivity constant of vacuum, and L is the gated nanowire length ($\approx$4 μm). In Eqs. (2) and (3), the transconductance is proportional to the gate-nanowire capacitance and is different between the nonembedded and embedded nanowire FETs in back-gate configuration [26]. For example, Wunnicke et al. have reported that for the nonembedded nanowire FETs, the capacitances are nearly two times lower than those for embedded nanowire FETs [26]. Thus, as shown in Figs. 2(c), 3(c), and 4(b), the passivated FETs have larger transconductances than those of the unpassivated devices, implying the stronger electrostatic gating effects for the FETs after passivation.

Consequently, based on the abovementioned results, the effects of surface roughness on the electrical characteristics of ZnO nanowire FETs before and after passivation can be demonstrated. For the unpassivated ZnO nanowire FET devices, the significant surface roughness of ZnO nanowires can cause the weak gating effects due to the physically poor contact between the ZnO nanowire and the dielectric layer, thereby, leading to poor electrical performance in the current on/off ratio and transconductance. On the other hand, for the passivated ZnO nanowire FET devices, the significant shifts in threshold voltages of rough ZnO nanowires can be attributed to the increased scattering effect and deep traps of channel electrons at the interfaces, that is, at the electrodes/ZnO nanowire and at the ZnO nanowire/insulating layers. Moreover, the rough ZnO nanowires have a larger surface area to volume ratio than the smooth ZnO nanowires and thus the surface depletion region due to the trap of electrons at the interfaces will occupy more significant fraction of the ZnO nanowires with smaller diameter than ZnO nanowires with larger diameter. Since the roughness and size of nanowires have considerable influence in the electronic transport of ZnO nanowire FETs, the control of the surface roughness and size of nanowires will be important for the application of the nanowire-based electronic devices.

4. Summary and conclusions

In summary, we have systematically investigated the effects of surface roughness on the electrical characteristics of ZnO nanowire FETs before and after passivation by PMMA. Electrical characteristics such as the threshold voltage shift and transconductance before and after passivation were strongly influenced by the surface morphology of ZnO nanowires. The FET devices that used rough ZnO nanowires showed significant changes in threshold voltage and transconductance before and after passivation, compared with those using smooth ZnO nanowires. Furthermore, both unpassivated- and passivated-FET devices that used smooth ZnO nanowires exhibited depletion-mode behaviour, whereas the FETs that used rough ZnO nanowires exhibited depletion- and enhancement-mode behaviours before and after passivation, respectively. In particular, the surface passivation of the FETs using rough ZnO nanowires is necessary to enhance their electrical properties due to the physically poor contacts induced by their rough surfaces.

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