Journal of
Nanoscience and Nanotechnology
Vol. 7, 1–5, 2007

Fabrication and Characterization of Directly-Assembled ZnO Nanowire Field Effect Transistors with Polymer Gate Dielectrics

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We report the fabrication and electrical characterization of ZnO nanowire field effect transistors (FETs). Dielectrophoresis technique was used to directly align ZnO nanowires between lithographically prepatterned source and drain electrodes, and spin-coated polyvinylphenol (PVP) polymer thin layer was used as a gate dielectric layer in "top-gate" FET device configuration. The electrical characteristics of the top-gate ZnO nanowire FETs were found to be comparable to the conventional "bottom-gate" nanowire FETs with a SiO_2 gate dielectric layer, suggesting the directly-assembled nanowire FET with a polymer gate dielectric layer is a useful device structure of nanowire FETs.

Keywords: ZnO Nanowire, Dielectrophoresis, Polymer Gate Dielectrics.

1. INTRODUCTION

In the near future physical and economic constraints are expected to limit the continued miniaturization of electronic and optical devices based on the current 'top-down' lithography-based technologies. Consequently, non-lithographic methods for synthesizing and organizing materials on the nanometer-scale are required. One-dimensional structures such as nanotubes and nanowires are expected to play a role as both devices and interconnect in future integrated circuits. Nanowires can be used for efficient transport of electrons and optical excitations, and are thus expected to be critical to the function and integration of nanoscale devices.[1]

Earlier research of nanowires has been based on random dispersion of nanowires from solution on device-structured substrates. A major problem in the realization of electronic circuits was hard to connect or assemble nanowires to metal electrodes, i.e., to position and contact them in proper places in a controlled way. Controlled assembly is essential for reliable fabrication. Several methods, for example, directed growth of nanowire and dip-pen nanolithography have been developed to assemble nanostructures to the electrodes.[2–4]

Among the controlled assembly techniques, dielectrophoresis (DEP) method is very simple and useful technique for spatial control of nanowire positioning because it does not require expensive equipment, high temperature, or chemical reaction. Moreover, the DEP technique is a method for controlled assembly of nanowires on microscale patterns, which provides the possibility to be scaled to wafer-level manufacture associated with large-scale nanowire-based electronics.

The electrical properties of semiconducting nanowires have been typically characterized with field effect transistor (FET) device structures. And, such nanowire FETs have been routinely fabricated as so-called "bottom-gate" FET device configuration (Fig. 1(b)), where highly doped Si substrate serves as a common bottom-gate electrode and SiO_2 layer serves as a gate insulating dielectric layer. In this bottom-gate configuration, nanowires are directly exposed to air if without any particular passivation layer. Then, semiconductor nanowires may be affected by exposure to ambient since oxygen molecule has influence on the electrical performance of nanowires.[5,6] In the contrast, in the "top-gate" device configuration (Fig. 1(d)), nanowires are completely covered by a dielectric layer and prevented them from being exposed to air. Especially, as compared with SiO_2 and Si_3N_4 dielectric layers, polymer dielectric layers can be easily deposited on substrates by spin-coating because it does not require vacuum equipment or high temperature process. Furthermore, polymer dielectric layers can exhibit quite a good electronic performance comparable to those inorganic gate dielectric materials, especially in terms of leakage current.[7–9]

In this study, we fabricated ZnO nanowire FETs using a polymer dielectric layer in the top-gate structure, where

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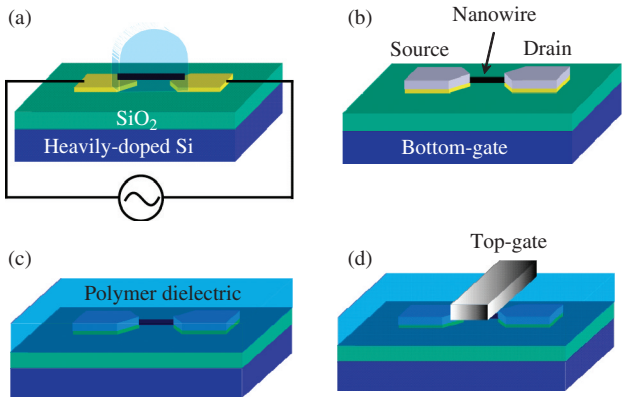

Fig. 1. Schematic diagrams of experimental procedure. (a) Direct assembly of nanowires by the dielectrophoresis method, (b) second metallization for source and drain electrodes, (c) deposition of a polymer gate dielectric layer, (d) fabrication of top-gate electrode. Bottom-gate configuration (b) and top-gate configuration (d).

ZnO nanowires were directly assembled between the source and drain electrodes by the DEP method. We used the cross-linked polyvinyl phenol (PVP) layer as a polymer gate dielectric layer. The top-gate ZnO nanowire FETs were characterized and compared with the bottom-gate ZnO nanowire FETs.

2. EXPERIMENTAL DETAILS

2.1. Dielectrophoretic Alignment of ZnO Nanowires

In this experiment, ZnO nanowires were synthesized on sapphire substrates by a vapor-solid-liquid process in a high temperature horizontal furnace system.[10] The synthesized ZnO nanowires were removed from the sapphire substrate and well dispersed in ethanol solution by sonication for 5 min. Then, individual ZnO nanowires were assembled across prepatterned electrodes of the device substrates with bottom-gate configuration using dielectrophoresis (DEP) technique.[11, 12] As device substrates, heavily B-doped silicon substrate with resistivity of 0.005–0.01 Ω cm, covered with 300 nm thick thermally grown silicon oxide was used. The prepatterned source and drain electrodes were made by evaporating Al (40 nm) on SiO_2/Si substrate and defined with standard photolithography. For the DEP assembly of nanowires, ethanol solution containing dispersed ZnO nanowires was dropped to the gaps between the prepatterned electrodes using micropipette. The gap distance between the prepatterned electrodes were made as 6–10 μm. Then, an AC voltage signal (5 V_{pp} at 1 MHz) was applied between the electrodes; this signal condition has been reported for optimizing the alignment of individual nanowires.[13] Figure 1(a) shows the schematic diagram of the experiment. The AC signal generates an alternating electrostatic force on the nanowires in the solution. By DEP force effect, the nanowires tend to align to the electrodes. An example of

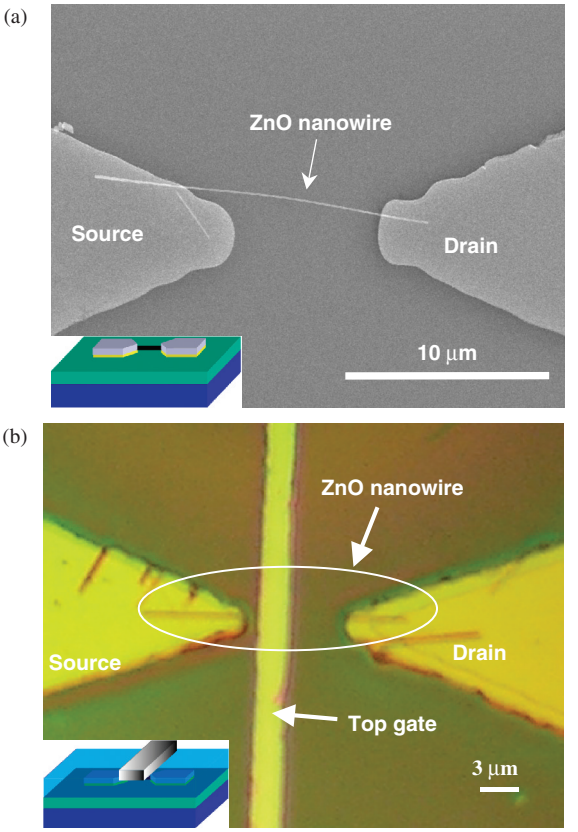

Fig. 2. (a) SEM image of assembled ZnO nanowire in bottom-gate configuration. (b) Optical microscope image of top-gate ZnO nanowire FET with a polymer gate dielectric layer.

such alignment of ZnO nanowire is shown in Figure 2(a). In this DEP assembly technique, the nanowires are simply placed on top of the electrodes, so that the contact resistance between the electrodes and nanowires may be high due to the poor contact between them. To improve the electric contact, we deposited another metal layer (Au/Ti; 70 nm/30 nm) on top of the prepatterned electrodes and the aligned nanowire (Fig. 1(b)). If we stop the fabrication at this stage, the device is called the bottom-gate configuration nanowire FET.

2.2. Fabrication of Top-Gate Structures with Polymer Gate Dialectic

For the gate insulator, we used cross-linked polyvinylphenol (PVP). The usage of PVP as a gate dielectric layer on Si wafer has been reported previously.[8] The PVP organic gate dielectric material consists of PVP polymer, poly(melamine-*co*-formaldehyde) as a cross-link agent (CLA), and propylene glycol monomethyl ether acetate (PGMEA) as a solvent. We used a mixed solution (PVP organic gate dielectrics) with an optimum ratio of components (10 wt% of PVP mixed with 5 wt% of CLA in 100 wt% of PGMEA). The mixed solution of PVP dielectrics was deposited by spin-coating on assembled nanowire FET

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device, followed by baking on a hot plate at 100 °C for 1 min and subsequent curing at 200 °C for 5 min. During the curing, the cross-link agent additive causes the PVP to be cross-linked, making the polymer film robust against exposure to acetone, PGMEA, and photoresist developer. The thickness of polymer film was found as ~200 nm from atomic force microscopy study. After the polymer deposition, gate electrode was made by evaporating Al (100 nm) and lift-off process. Finally, the transistor properties of top-gate ZnO nanowire FETs with polymer gate dielectric (Fig. 1(d)) were measured by a semiconductor parameter analyzer (HP4155C).

3. RESULTS AND DISCUSSION

The attraction and alignment of objects such as nanotubes or nanowires towards the electrodes are caused by a dielectrophoresis (DEP) force $\vec{F}$, approximately given by[14]

$$\vec{F} \propto \varepsilon_1 \mathrm{Re}\left(\frac{\varepsilon_2^* - \varepsilon_1^*}{\varepsilon_2^* + 2\varepsilon_1^*}\right)\vec{\nabla}|\vec{E}|^2 \quad (1)$$

Here, ε_2^* and ε_1^* are the complex dielectric constants of the nanowire and solvent medium, respectively, and $\vec{E}$ is the external electric field. During the dielectrophoresis alignment, the orientation of nanowires is controlled by the torque $\vec{T}$, exerted on the induced electrical dipole moment,[15]

$$\vec{P} = q\vec{d} \quad (2)$$

where q is the induced electrical charge on the nanowire and $\vec{d}$ is the displacement between the induced charges. When the nanowires are moved toward the electrode, the direction of movement is along the radial direction of electrode. If the length of a nanowire is longer than the gap between two electrodes, it can be assembled across two elecrodes.[15]

Figure 2(a) is a scanning electron microscope (SEM) image of directly assembled ZnO nanowire across the source and drain electrodes by the DEP method. This device structure belongs to the bottom-gate configuration since highly doped Si substrate was used as a common bottom-gate electrode (Fig. 1(b)). The transistor characteristics of the bottom-gate ZnO nanowire FET were obtained as shown in Figure 3. Figure 3(a) is the source–drain current versus voltage ($I_D - V_{DS}$) curve at different gate voltages in the range from 0 to 10 V with 2 V step. Figure 3(b) is source–drain current versus gate voltage ($I_D - V_G$) at different source–drain voltage in the range from 100 to 500 mV with 100 mV step. The modulation of the channel conductance indicates that the operation of the device is the typical n-type semiconducting behavior, since the current increases with increasing positive gate voltage, whereas it decreases with increasing negative gate voltage. It is well known that the undoped ZnO generally exhibits n-type conduction due to the presence of intrinsic donor-type defects induced by deviation from stoichiometry.[16, 17]

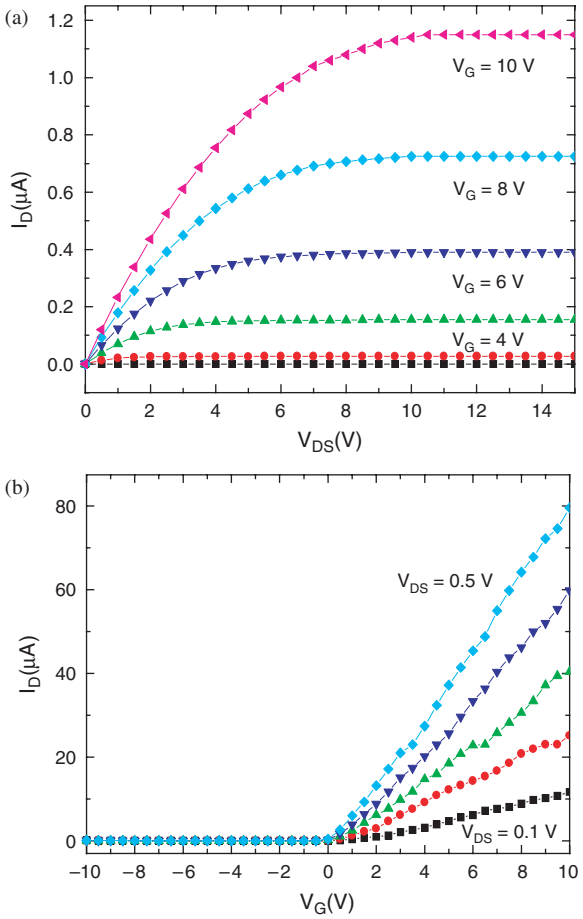

Fig. 3. $I_D - V_{DS}$ characteristics (a) and $I_D - V_G$ characteristics (b) of bottom-gate ZnO nanowire FET.

Carrier concentration of ZnO nanowire can be estimated from total charge, $Q = C|V_G - V_{th}|$, where C is the capacitance of nanowire with respect to the gate insulator and V_{th} is magnitude of the threshold voltage. Using the cylinder-on-plate model, the nanowire capacitance is given by[18]

$$C = \frac{2\pi\varepsilon\varepsilon_o L}{\cosh^{-1}(1 + t_{ox}/r)} \quad (2)$$

where ε is the dielectric constant of SiO_2, L is channel length of nanowire FET, r is the radius of ZnO nanowire, t_{ox} is the SiO_2 thickness. Using $\varepsilon = 3.9$, $r = 50$ nm, $t_{ox} = 300$ nm, $L = 8$ μm, and $V_{th} = 0.2$ V, the carrier concentration at $V_G = 2$ V was found as $\sim 1.2 \times 10^{17}$ cm^{-3}. And the carrier mobility can be calculated with the following equation[19]

$$\mu = \frac{L^2}{CV_{DS}}\frac{dI_{DS}}{dV_G} \quad (3)$$

where dI_{DS}/dV_G is transconductance that is the slop of linear region of $I_D - V_G$ curve. Transconductance (dI_{DS}/dV_G) was found as 8 nS at $V_{DS} = 500$ mV, and the mobility was determined to be ~16 cm^2/Vs.

We also fabricated top-gate ZnO nanowire FETs with PVP polymer gate dielectric layer as device structure

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shown in Figure 1(d). Figure 2(b) is an example optical microscope image of such top-gate nanowire FET. The width of the top-gate electrode is 3μm. A ZnO nanowire (circled in Fig. 2(b)) exists underneath the PVP polymer gate dielectric layer. The transistor characteristics of the top-gate ZnO nanowire FET were also measured and are summarized in Figure 4. Similar to Figure 3, Figure 4(a) is the source–drain current versus voltage ($I_D - V_{DS}$) curve at different gate voltages in the range from 0 to 10 V with 2 V step, and Figure 4(b) is the source–drain current versus gate voltage ($I_D - V_G$) at different source–drain voltage in the range from 100 to 500 mV with 100 mV step.

We also calculated carrier concentration and mobility in the top-gate nanowire. In this top-gate configuration, channel length L is same as the width of the top-gate electrode (3 μm), t_{ox} is the thickness of the polymer gate dielectric (200 nm), and ε is the dielectric constant of cross-linked PVP (3.6).[7] Using these values and transconductance of 10.6 nS at $V_{DS} = 500$ mV, the carrier concentration at $V_G = 2$ V was found as $\sim 4.9 \times 10^{16}$ cm^{-3}, and the mobility was found as ~ 8 cm^2/Vs. As summarized in Table I, the characteristics of the top-gate FET with a polymer gate dielectric layer are comparable to those of the bottom-gate device. In particular, the carrier concentration of the bottom-gate FET was found about five times larger than that of the top-gate FET and the transconductance of top-gate nanowire FET was found slightly larger than that of bottom-gate nanowire FET although the difference is not dramatic. This tendency is due to the gating effect by the local top-gate electrode. Similar effect has been reported for the case of local top-gate electrode for carbon nanotube FETs.[20]

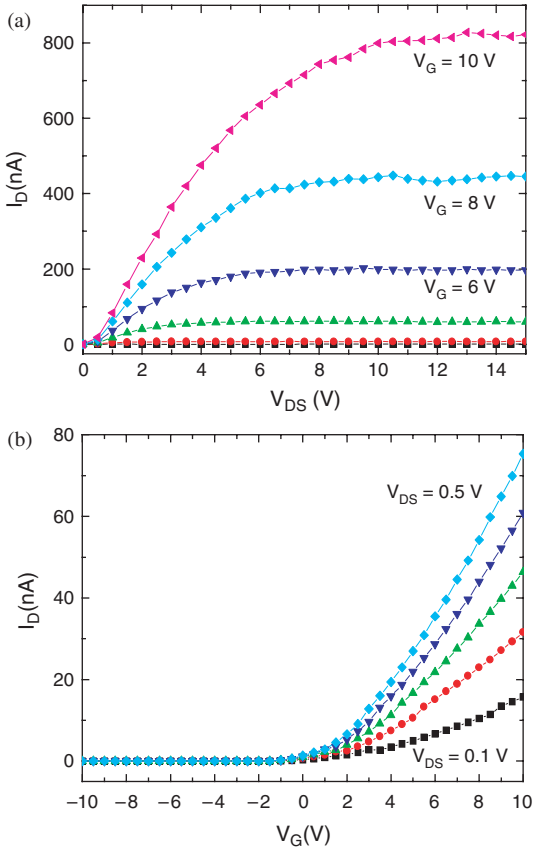

Fig. 4. $I_D - V_{DS}$ characteristics (a) and $I_D - V_G$ characteristics (b) of top-gate ZnO nanowire FET with a polymer gate dielectric layer.

Table I. Summary of the electrical parameters for ZnO nanowire FETs.

Configuration	V_{th} (V)	n (cm^{-3})	μ (cm^2/Vs)
Bottom-gate	0.2	1.2×10^{17}	16
Top-gate	1.3	4.9×10^{16}	8

4. CONCLUSIONS

A simple dielectrophoresis technique was used to directly assemble ZnO nanowires on transistor device substrates. A cross-linked polyvinylphenol (PVP) layer was used as a gate insulating dielectric layer in the top-gate nanowire transistor configuration. The electrical characteristics of the top-gate configuration ZnO nanowire transistors were found comparable to the conventional type of the bottom-gate nanowire transistors, which demonstrate the combining controlled assembly of nanowires with a polymer gate dielectric layer can provide useful device structure for nanowire field effect transistors.

Acknowledgments: This work was supported by the Brain Korea 21 Project, Proton Accelerator User Program of Korea, and the Program of Integrated Molecular Systems at GIST.

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Received: 17 April 2007. Revised/Accepted: 18 May 2007.