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Nano-Scale Memory Characteristics of Silicon Nitride Charge Trapping Layer with Silicon Nanocrystals

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Silicon nanocrystals (Si-NCs) embedded in a silicon nitride (SiN) layer were fabricated as a charge trapping layer for nonvolatile memory (NVM) device applications. Nano-scale memory characteristics were investigated using conductive atomic force microscopy (C-AFM) and a semiconductor parameter analyzer. Nano-scale memory characteristics of Si-NCs embedded in the SiN layer were obtained from the shift of the current–voltage (I–V) curve. Charge trapping/detrapping and multi-level charge storage in Si-NCs embedded in the SiN layer were obtained at a metal–oxide–semiconductor (MOS) structure of about 100 nm^2 at room temperature. The flat band voltage (V_{FB}) shift was about 0.37 V, which is agreed well with the calculated V_{FB} shift for one electron per nanocrystal. [DOI: 10.1143/JJAP.45.L807]

KEYWORDS: SONOS, nonvolatile memory, C-AFM, Si nanocrystal, nano-scale memory

Silicon–oxide–nitride–oxide–silicon (SONOS) type devices are strong candidate for nonvolatile memory (NVM) devices due to their lower program/erase (P/E) voltage, faster P/E speeds, better scalability, and reliability characteristics compared to other types of memory devices.[1–3] In spite of these strengths as NVM devices, efforts are needed to improve both P/E speed and the long term retention. In particular, optimization of the thickness of each layer and increasing the charging capacity constitute the main approaches for obtaining better memory characteristics. Recently, silicon nanostructures have been the subject of intensive study in the field of electric devices such as single electron transistor, switching devices, and memory devices.[4,5] Notably, a field effect transistor structure with silicon nanocrystals (Si-NCs) embedded in the gate oxide has been widely investigated in relation to memory devices.[6]

In order to increase the charge trapping efficiency, intensive effects have been made to develop a charge trapping layer with large density and deep trap sites. From this point of view, formation of Si-NCs in the charging trapping layer has been employed to enhance the charge trapping efficiency. In our previous works, we fabricated micro-scale SONOS type devices that contain Si-NCs embedded in a silicon nitride (SiN) layer formed by plasma immersion ion implantation (PIII) and thermal annealing method. These devices showed excellent electrical characteristics for NVM devices.[7] However, because of the random distribution of Si-NCs embedded in the SiN layer, it is necessary to confirm the nano-scale electrical characteristics of this layer.

It is difficult to characterize a nanoscale device using microelectronic electrical characterization techniques. Therefore, some special characterization tools are strongly required to reveal the device's nano-scale electrical characteristics. Recently, conductive atomic force microscopy (C-AFM) technique has been widely used to study the localized current conduction phenomena and to estimate the amount of charges in gate insulators.[8–10] Because C-AFM can be employed on a bare oxide surface, nanoscale memory characteristics can be measured easily without complicated sample preparation. In this paper, using C-AFM, we investigated memory characteristics of a SiN charge trapping layer with Si-NCs in relation to nano-scale NVM device applications.

After the standard cleaning process of the p-type silicon wafer, 25-Å-thick SiO_2 was thermally grown and 130-Å-thick SiN film was deposited by low-pressure chemical vapor deposition (LPCVD). Excess silicon in the SiN layer was formed by a low energy PIII system using SiH_4 gas at 500 eV with a Si^+ dose higher than 10^{16} cm^{-2}. In order to form Si-NCs in the charge trapping layer, furnace annealing at 1000 °C for 90 min was preformed in N_2 ambient. Average diameter of approximately 3.5 nm and estimated mean density of 2×10^{12} cm^{-2} were determined by cross-section transmission electron microscopy. A 60-Å-thick SiO_2 blocking layer was deposited by LPCVD. In order to the measure electrical properties of the as fabricated SONOS type structure of 10^4 μm^2, an n^+ polycrystalline silicon gate electrode was deposited followed by annealing in conventional forming gas. Other detailed conditions and confirmations of formation of Si-NCs in the SiN layer were described previously.[7]

A C-AFM measurement system, which is composed of a commercial AFM (XE-100, PSIA) and a semiconductor parameter analyzer, was used to evaluate the nano-scale memory characteristics.[11] A conductive tip coated with titanium (Ti) and platinum (Pt) was placed in direct contact with the blocking oxide surface. Current flowing between the conductive tip and sample was measured by a HP4155A semiconductor parameter analyzer.

Figure 1(a) shows the capacitance–voltage (C–V) hysteresis curve of as fabricated micro-scale SONOS type devices containing Si-NCs embedded in a SiN layer as a charge trapping layer. A sweep rate of 0.05 V s^{-1} and holding time of 1 s were sufficient for charging and discharging in Si-NCs. Large width of counterclockwise C–V hysteresis curves with large widths were obtained with increasing sweep bias range, indicating the electron injection from the substrate to the charge trapping layer. SONOS device Si-NCs in SiN shows large memory window of 5 V at +9 V/−9 V for P/E. However, it is difficult to observe V_{FB} shift at nano-scale devices, because the capacitance value, which is proportional to the contact area, too low. In the

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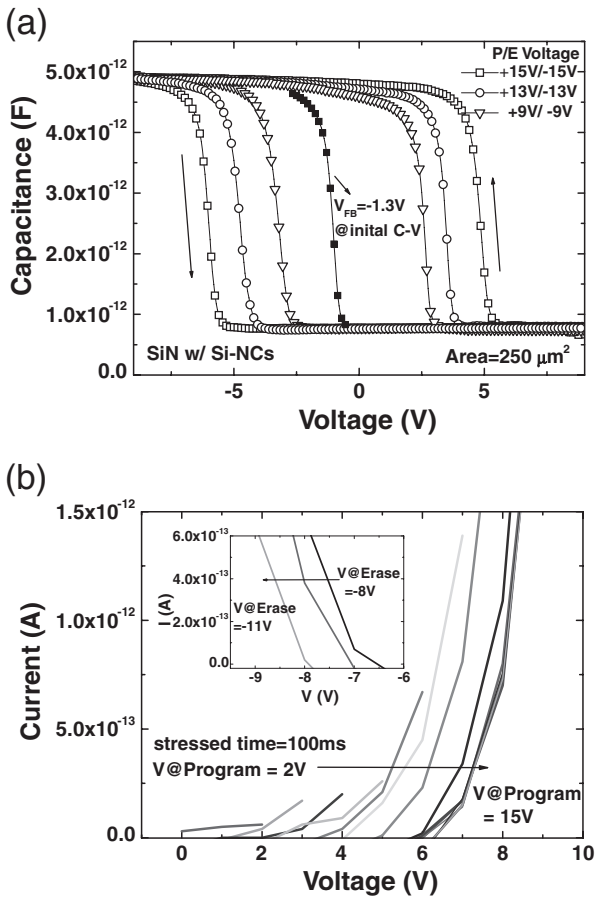

Fig. 1. (a) *C–V* hysteresis curve of SiN with Si-NCs for different program/erase voltage and initial *C–V* (b) shift of *I–V* curve for different program voltage at a gate of $100 \times 100\,\mu m^2$. Inset of (b) shows shift of *I–V* curve for different erase voltages.

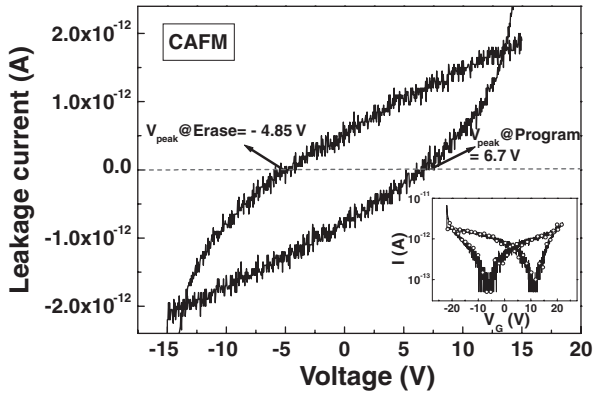

Fig. 2. *I–V* hysteresis curve at a gate of about $100\,nm^2$. *I–V* hysteresis was measured by C-AFM. The inset shows the absolute value.

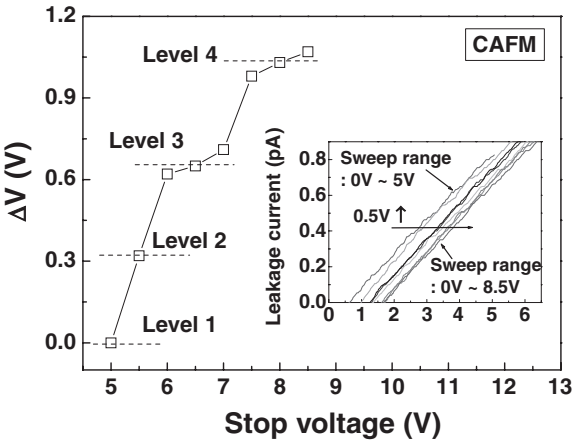

Fig. 3. Room temperature multi-level charge storage in silicon nanocrystals incorporated in silicon nitride at a gate area of $100\,nm^2$. The inset shows the *I–V* measurement that was performed from 0 V to different stop voltages.

nanometer scale area, the capacitance value is in the femtofarad level. This value is too small to measure and thereby obtain the *C–V* hysteresis, using a conventional HP 4284 LCR meter. Therefore, another method to analyze the charge trapping behavior of nanoscale device is needed.

Figure 1(b) shows the shift in current–voltage (*I–V*) curves at a $10^4\,\mu m^2$ area. Voltage sweep was performed from 0 V to different program volts. Positive shifts of the *I–V* curves were observed as the program voltage was increased. The inset figure shows V_{FB} shifts in the *I–V* curves according to the erase voltage. Gate voltage (V_G) is a function of induced charge (Q_S), as shown in eq. (1)[12)]

$$V_G = V_{FB} - \frac{Q_S}{C_i} + \phi_S \quad (1)$$

Here, C_i is the insulator capacitance and ϕ_S is the surface potential. During program mode, a negative induced charge was formed by electron trapping while during erase mode, electron detrapping and hole trapping formed a positive induced charge. In the case of program, when electrons are trapped in the charge trapping layer, the magnitude of oxide filed become lower. To obtain the same current flow, large voltage is needed. Consequently, the shift of voltage corresponds with the amount of trapped electrons. Consistently, *I–V* characteristics shows the voltage shift measured after the biasing program voltage, i.e., the amount of trapped electrons.

I–V hysteresis curves measured at a gate area of $100\,nm^2$ are shown in Fig. 2. *I–V* hysteresis measurement was performed from negative voltage to positive voltage (forward sweep) and *vice versa* (reverse sweep). Counterclockwise *I–V* hysteresis was obtained. During the forward sweep, the device was erased by negative voltage and showed a negative shift. In the reverse case, the device showed a positive shift, according to the applied program voltage. The inset of Fig. 2 shows the peak shift of the *I–V* curve. In order to determine the amount of the trapping charge, we compared the peak voltages (V_{peak}) that show zero current at forward and backward sweep. At a P/E voltage of $+15\,V/-15\,V$, the values of V_{peak} of erase and program were -4.85 and 6.7 V. The amount of V_{peak} shift in the *I–V* curve using C-AFM is consistent with the amount of V_{FB} shift at *C–V* hysteresis.

Figure 3 shows multi-level charge storage in Si-NCs embedded in SiN at room temperature (RT). It was measured by the voltage shift in program mode by sweeping from 0 V to different program voltage. The *I–V* curve shows a parallel shift in the positive direction, as shown in the inset of Fig. 3. The amount of voltage shift is shown in Fig. 3, which shows well controlled multi-level charge storage. Two or three Si-

NCs in a gate area of $100\,\mathrm{nm}^2$ might serve as more dominant charge traps than a SiN trap and thus a discrete level of charge storage can be possible. V_{FB} shift (ΔV_{FB}) for a single electron per nanocrystal is given by:[6)]

$$\Delta V_{FB} = \frac{q n_{well}}{\varepsilon_{ox}} \left(t_{cntl} + \frac{1}{2} \frac{\varepsilon_{ox}}{\varepsilon_{si}} t_{well} \right) \quad (2)$$

Here, n_{well} is the density of nanocrystals, t_{cntl} is the thickness of the control oxide, and t_{well} is the linear dimension of the nanocrystals well. The calculated V_{FB} shift for one electron per nanocrystal is about 0.37 V and was in good agreement with our results. This indicates that the gate voltage shift for each level is caused by single electron charging in a Si-NC.

In conclusion, memory characteristics of high density Si-NCs incorporated in SiN as an alternative charge trapping layer were investigated using C-AFM at a gate area of $100\,\mathrm{nm}^2$. A SiN trapping layer with Si-NCs has additional charge trapping sites and thus the fabricated device showed a large memory window. It was possible to observe charge trapping characteristics by the flat-band voltage change from I–V measurement. Multi-level charge trapping/detrapping was also obtained at RT through C-AFM.

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